Model V385-EA11/EB11

16-Channel Digital Input/Output

INSTRUCTION MANUAL

March, 1998

CONTENTS

FIGURES

TABLES

16-channel Digital Input/Output

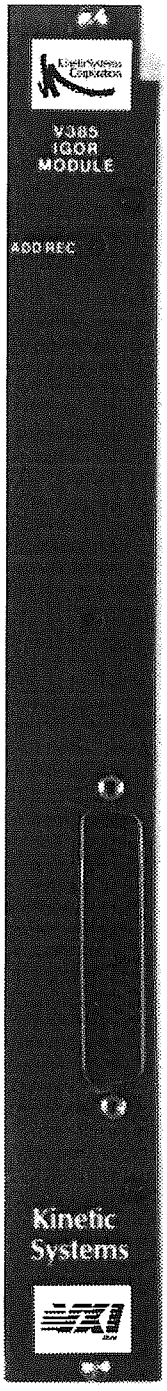
Provides general-purpose interfacing of TTL or HTL signals **V385**

Features

- **16-bit I/O with handshaking**
- **Four control pulses and one status bit**
- *** Complete interrupt capability**
- **HTL and TTL signal options available**

Typical Applications

- **Test cells**
- **Accelerator control systems**
- **Interfacing to subsystems requiring digital monitoring and control**



General Description *(Product specifications and descriptions subject to change without notice.)*

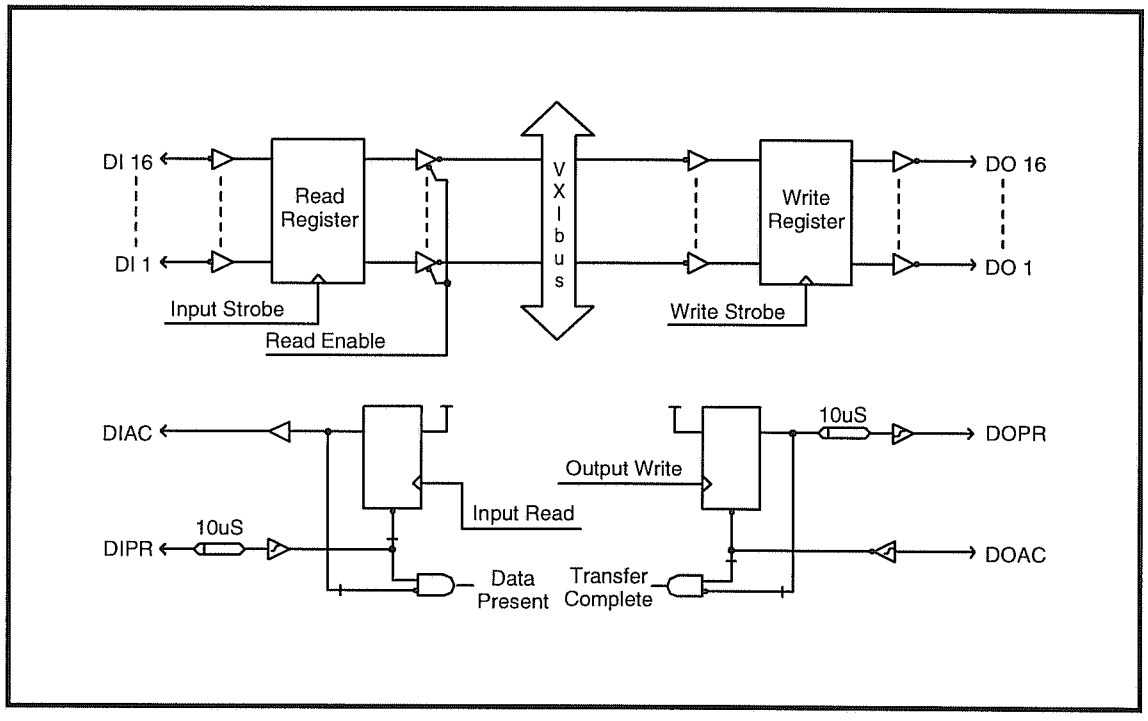
The V385 is a single-width, C-size, register-based, VXIbus module containing a 16-bit input gate, a 16-bit output register, a 1-bit status input, and four 500 ms pulse outputs. Full handshaking is provided for the input gate and output register. The handshaking signals can be tested; they can also generate an interrupt. The module can be used without handshaking, if desired.

Each of the four pulsed control outputs can drive loads up to 100 mA and +24 V. The V385 can be ordered with all external signals using high threshold logic (HTL) or TTL interfaces. With the HTL option, the data and status inputs recognize a logic "1" as being 1 to 6 V, and a logic "0" as being 8 to 15 V.

Commands are available for writing the entire 16-bit output register, for writing eight bits at a time, and for writing four bits at a time. This allows the module to drive independent 4-bit or 8-bit devices.

All I/O signals are brought to a 50-contact "D" type connector on the module's front panel.

The V385 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.



Item	Specification
Number of Channels	32: 16 inputs, 16 outputs
Data Inputs	
Input voltage	
TTL option	0-5 V
HTL option	0-15 V
Low-level input current	
TTL option	1 mA
HTL option	1 mA
Switching threshold	
TTL option	+2 V
HTL option	+7 V
Data Outputs	
Output voltage	
TTL option	0-5 V
HTL option	0-15 V
Output sinking current (V_o = 0 Volts)	
TTL option	30 mA
HTL option	30 mA
Switching threshold	
TTL option	+2 V
HTL option	+7 V
Output Control Pulses Width	500 ms
I/O Connector Type	50P "D"
Mating connector	KineticSystems Model 5934-Z1A
Power Requirements:	
+5 V	1.8 A, typical
+24 V (HTL option only)	50 mA, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to +40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V385-EA11 16-channel Digital Input/Output; TTL-level signals
Model V385-EB11 16-channel Digital Input/Output; HTL-level signals

Related Products

Model 5851-Bxyz Cable—50S "D" to Unterminated
Model 5851-Dxyz Cable—50S "D" to 50S "D"
Model 5851-Exyz Cable—50P "D" to 50S "D"
Model 5934-Z1A Connector—50S "D"

UNPACKING AND INSTALLATION

The Model V385 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V385 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V385 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the modules right-side ground shield. Refer to FIGURE 1.)

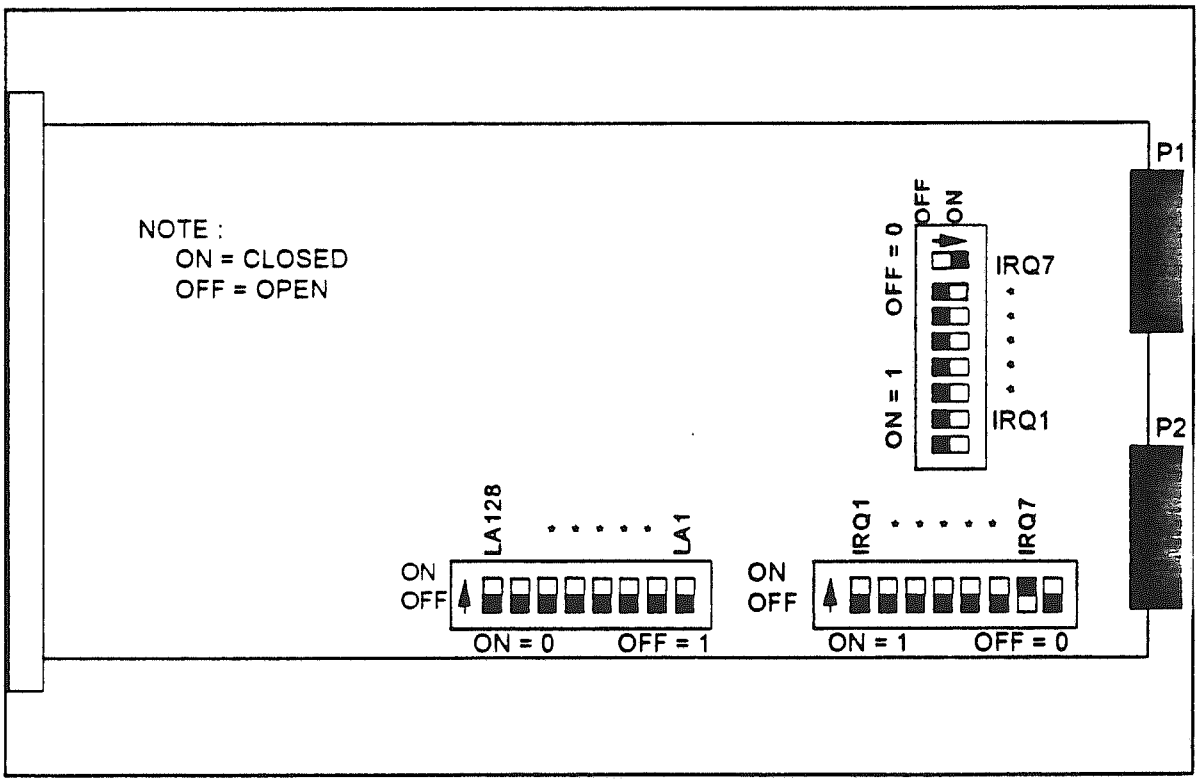


FIGURE 1 - V385 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to "1" (VXI defined).

Bits 13 through 6 are user-selectable via the address switches LA128-LA1.

Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V385 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 (page 3) for the switch locations and switch settings. Both banks of eight-position switches must be set the same. As shown in Figure 1 (page 3) IRQ 7 is set to the same position in both banks.

Module Insertion

The V385 is a C-sized, single width VXIbus module. It requires 1750 milliamperes of +5 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE IN THE BACKPLANE

To insure proper interrupt acknowledge cycles from the V385 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V385 and the Slot 0 Controller.

FRONT PANEL INFORMATION

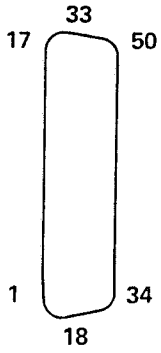
LEDs

ADD_REC This LED is illuminated when the operational registers are accessed.

CONNECTORS

The front panel I/O connector is a 50-contact "D" connector and is used to connect the digital inputs and outputs to a peripheral device. Refer to Table 1 (see below) for pin assignments.

TABLE 1 - V385 CONNECTOR PINOUT ASSIGNMENTS



FACE VIEW

NOTES: Value shown is for HTL version (V385-EB11); for TTL version (V385-EA11), a +5 volt, 1A signal is provided.

Pin/Wire List

50 PIN 'D'

PIN NO.		PIN NO.		PIN NO.	
17	DI 16	33	DO 16	50	GND
16	DI 15	32	DO 15	49	+24V, 0.5A
15	DI 14	31	DO 14	48	+15V, 0.25A (NOTE 1)
14	DI 13	30	DO 13	47	OFF D
13	DI 12	29	DO 12	46	ON C
12	DI 11	28	DO 11	45	OFF B
11	DI 10	27	DO 10	44	ON A
10	DI 9	26	DO 9	43	GND
9	DI 8	25	DO 8	42	DOAC
8	DI 7	24	DO 7	41	GND
7	DI 6	23	DO 6	40	DOPR
6	DI 5	22	DO 5	39	GND
5	DI 4	21	DO 4	38	DIAC
4	DI 3	20	DO 3	37	GND
3	DI 2	19	DO 2	36	DIPR
2	DI 1	18	DO 1	35	GND
1	GND (0V)			34	Status Bit (TST)

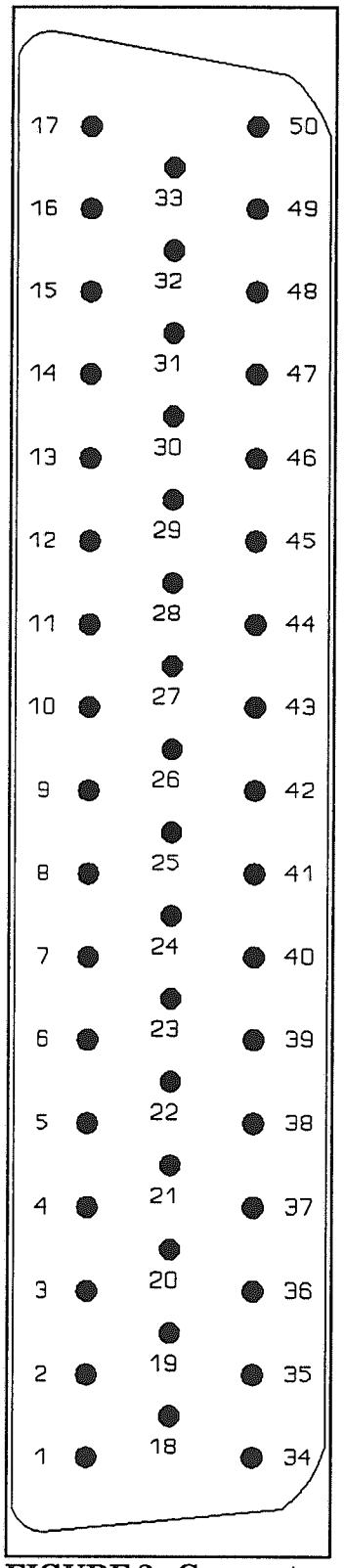


FIGURE 2 - Connector Pinout

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V385 implements those required for register-based devices. The V385 also contains a set of Operational Registers to monitor and control the functional aspects of the devices. Both registers sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of C000 hex to FFC0 hex.

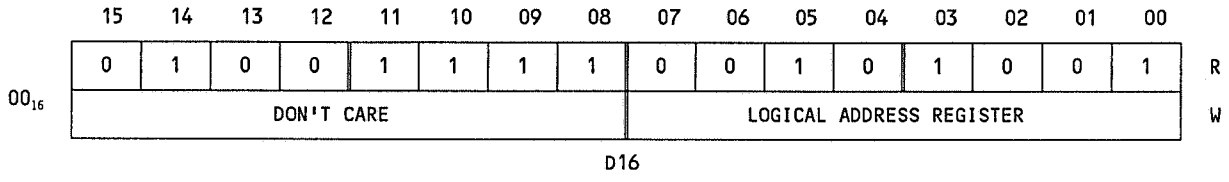
VXIbus Configuration Registers

Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V385 are offset from the base address. Note: the V385 only responds to these addresses if the Short Nonprivileged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle. Table 2 shows the applicable Configuration Registers present in the V385, their offset from the base (Logical) address, and their Read/Write capabilities.

TABLE 2
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET (HEX)	W/R MODE	REGISTER NAME
00_{16}	W/R	ID/Logical Address Register
02_{16}	R	Device Type Register
04_{16}	W/R	Status/Control Register
06_{16}	W/R	Offset Register
08_{16}	R	Attribute Register
$1E_{16}$	R	Subclass Register

ID/Logical Address Register (offset 00_{16})



On READ transactions:

Bit(s)	Mnemonic	Meaning
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V385. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

Device Type (OFFSET 02_{16})

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	1	1	1	1	0	0	1	1	0	1	0	0	0	1	0	1	R
	D16																

On READ transactions:

Bit(s)	Mnemonic	Meaning
15 - 12	Required Memory	The V385 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model V385 (385_{16}).

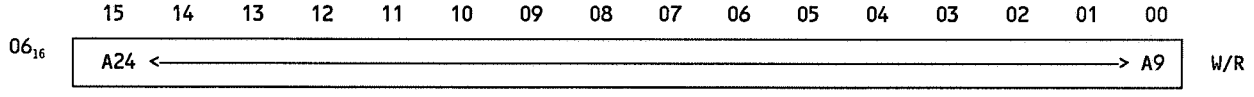
Status/Control Register (OFFSET 04_{16})

15	14	13	12	11 10 09 08 07 06 05 04	03	02	01	00
A24 ACT	MODID	S	1	ZEROs	RDY	PASS	0	RST
A24 ENA	N/U	N/U	1	NOT USED				RST

Bit	Mnemonics	Description
15	A24	Writing a "1" will enable A24 addressing and allow access to the Operational Registers. Reading a "1" indicates A24 is active. This bit is reset to a "0" on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on VXIbus

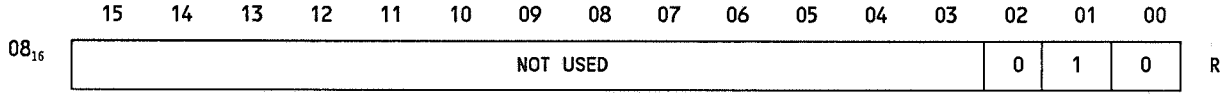
		connector P2. A "0" will indicate that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V385. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1".
11-4	N/U	Not used. Read as a "0".
3	RDY	READY. The V385 is always ready. Read as a "1".
2	PASS	PASS. The V385 will always pass self tests. Read as a "1".
1	N/U	NOT USED. Read as a "0".
0	RST	RESET. This Read/Write bit controls the Soft Reset condition within the V385. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Register (see below) except the Diagnostic and Interrupt Status registers is inhibited. The output bit pattern from the module are maintained in the state they were in just prior to the Soft Reset being enabled. This bit can be reset by writing a "0", on power-up or the assertion of SYSRESET*.

Offset Register (OFFSET 06_{16})



This 16-bit read/write register defines the base address of the A24 Operational Registers. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Attribute Register (OFFSET 08_{16})



Subclass Register (OFFSET $1E_{16}$)

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	R

Bit(s)	Mnemonic	Meaning
15	Extended Device	"1" indicates this to be a VXIbus defined Extended Device.
14-00	Register-Based	$7FFE_{16}$ indicates this to be an Extended register-based Device.

OPERATIONAL REGISTERS

The Operational Registers are the channel to access the functional registers of the V385. For compatibility with other KineticSystems VXIbus modules in this series, these registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register (see page xx). **Note: The V385 will only respond to these addresses if the Standard Nonprivileged Data Access (39_{16}), Standard Nonprivileged Program Access ($3A_{16}$), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for the bus cycle(s).**

Of the 256 bytes requested by the setting of the Device Type register in the Configuration Register set, only 62 bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type register.) Table 3 shows the applicable Operational Registers present in the V385, their offset from the base A24 address, and their Read/Write capabilities.

TABLE 3
V385 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

A24 OFFSET	W/R MODE	REGISTER NAME
00_{16}	W/R	Diagnostic Register
02_{16}	W/R	Interrupt Status/ID Register
12_{16}	R	Input Data Register
16_{16}	W	Output Data Register (Word)
$1A_{16}$	W	Output Data Register (Byte 1)
$1E_{16}$	W	Output Data Register (Byte 2)
22_{16}	W	Output Data Register (Nibble 1)
26_{16}	W	Output Data Register (Nibble 2)
$2A_{16}$	W	Output Data Register (Nibble 3)
$2E_{16}$	W	Output Data Register (Nibble 4)
32_{16}	R	Execute Pulse A
36_{16}	R	Execute Pulse B
$3A_{16}$	R	Execute Pulse C
$3E_{16}$	R	Execute Pulse D
42_{16}	R	Enable Read INT Request
46_{16}	R	Disable Read INT Request
$4A_{16}$	R	Enable Write INT Request
$4E_{16}$	R	Disable Write INT Request
52_{16}	R	Clear/Disable INT Status
56_{16}	R	Reserved
$5A_{16}$	R	Clear Read INT Status
$5E_{16}$	R	Clear Write INT Status
62_{16}	R	Test Read INT Request
66_{16}	R	Test Write INT Request
$6A_{16}$	R	Test Data Present INT
$6E_{16}$	R	Test Transfer Complete INT
72_{16}	R	Test Input Status Bit

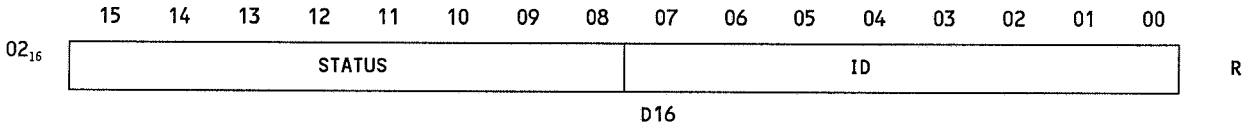
Diagnostic Register (OFFSET 00_{16})

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care								D	S	0	INT ENA	INT SRC	0	0	0	R
00_{16}	Don't Care								0	0	0	INT ENA	0			INIT	W
	D16																

Bit	Mnemonic	Description
15-8	N/U	Not Used. Read as "0".
7	Diagnostic	When this bit is set to a "1", the last register access to the operational registers (12_{16} through 72_{16}) was valid.

6	Status	When this bit is set to a "1", the last register access to the operational registers (12_{16} through 72_{16}) was accepted.
5	N/U	Not Used, read as "0".
4	INT ENA	Interrupt Enable: setting this bit to a "1" will enable interrupts.
3	INT SRC	Interrupt Source: When this bit is set to a "1", either there is input data available for the V385 to accept, or the module has completed the transfer of output data.
2,1	N/U	Not Used, read as "0".
0	INIT	Setting this bit to a "1" will only reset the operational registers (12_{16} through 72_{16}). The configuration registers and the Diagnostic register are unaffected.

Interrupt Status/ID Register (OFFSET 02_{16})



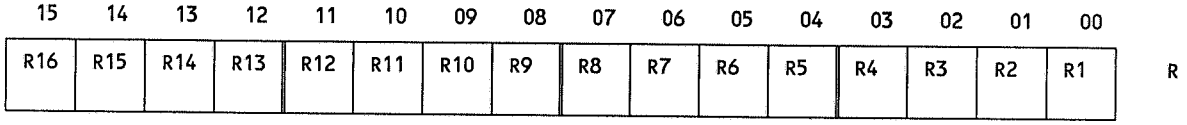
This is a read only 16-bit Interrupt Status Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value, as defined by the VXIbus specification.

Bit	Mnemonic	Description
15-8	STATUS:	These eight bits will indicate Request True or Request False. Request True = FD_{16} Request False = FC_{16}
7-0	ID:	These eight bits represent the Logical Address of the V385 Configuration Registers.

Input Register (OFFSET 12_{16})

This register will read input data to the V385. At the start of the read cycle, the contents of the data register are locked up to prevent any changes at the module front panel from

adversely affecting the read operation. The Input signals are low-true at either HTL (-EB11 option) or TTL (-EA11 option) level. The Input Gate can be used without handshaking, if desired. Handshaking can be used to coordinate the data exchange from the peripheral device. The status bit in the Diagnostic register will always be equal a one when this register is read. A read from this register will clear the read interrupt status bit. A register layout is given below:

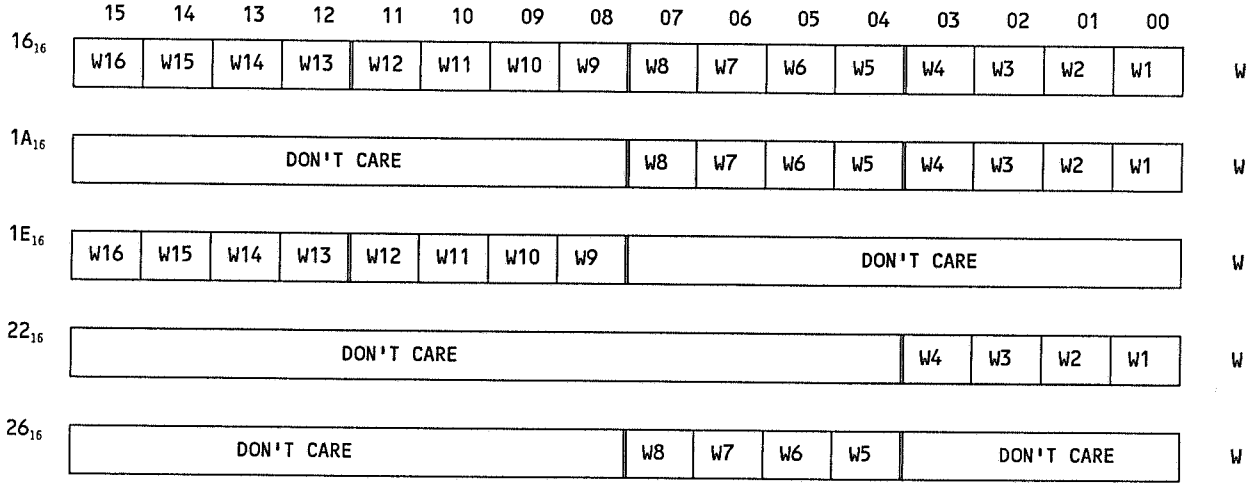


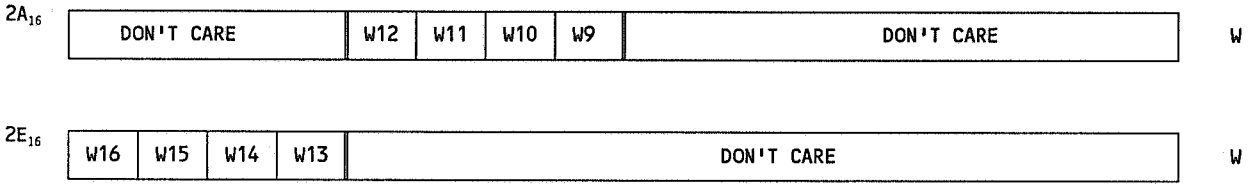
Output Registers

The Output register can be written using one of seven write functions to control the 16-bit output data. These write functions allow flexibility for occasions where more than one device can be part of the 16-bit word. For example, if V385 is to drive a single device with up to 16-bits, the register at offset 16_{16} is used to write the data word.

In some cases, it is desirable to control two separate devices (8-bits each). For these applications, the register at offset $1A_{16}$ writes the lower 8-bits and the register at offset $1E_{16}$ will write the upper 8-bits. To drive four 4-bit devices, the register at offset 22_{16} through $2E_{16}$ are used to control the appropriate four bits. Refer to Table 3 for the appropriate registers. Note that the byte and nibble write functions affect only the desired bits and leave all others bits unchanged. Also, the write lines to the data output bit mapping is the same for all commands.

The output signals are low-true at either HTL or TTL level. The output register can be used without handshaking, if desired. Handshaking can be used to coordinate the data exchange to the peripheral device. All seven write functions will clear the write interrupt status bit. The status bit in the Diagnostic register will always be equal to a "1" when any of the seven registers are written. A register layout is shown below:





OPERATIONAL CONTROL REGISTERS (OFFSET 32_{16} through 72_{16})

The V385 has seventeen Operational Control Registers at offset 32_{16} through 72_{16}. These registers are Read-Only and return a 16-bit data code. There are only two possible codes that can be returned. The first data code will return a value of zero and has the same meaning as the Status bit in the Diagnostic Register set to logical "0". The second data code will return a value of one and has the same meaning as the Status bit in the Diagnostic Register set to a logical "1". This data code will indicate the command was accepted or a test condition is true when equal to one. These sixteen Operation Control Register are described below:

Pulse Outputs

The V385 has four pulsed control outputs. These outputs are open-collector and diode-clamped to +24 volts. No pull-up resistors are provided on the module, but they can drive up to 100 mA at +24 volts. These outputs are generally used to turn peripheral devices ON or OFF. The following will indicate the polarity of the pulsed outputs.

Designation	Register Offset	Output State
ON -A-	32_{16}	LOW when pulsed
OFF -B-	36_{16}	HI when pulsed
ON -C-	$3A_{16}$	LOW when pulsed
OFF -D-	$3E_{16}$	HI when pulsed

The control pulse outputs are active for 0.5 seconds, typically when executing a controlled output pulse, a data code of one will indicate the command was accepted. A data code of zero will be returned if the same pulse was retriggered before the previous has completed.

Enable Read INT Request (OFFSET 42_{16})
Disable Read INT Request (OFFSET 46_{16})

A read from either register will enable or disable the Read Interrupt Request. The Interrupt Request must be enabled if the V385 is to set an interrupt when DIPR (Data In Present) becomes true. Both registers will return a data code of one.

Enable Write INT Request (OFFSET $4A_{16}$)
Disable Write INT Request (OFFSET $4E_{16}$)

A read from either register will enable or disable the Write Interrupt Request. The Interrupt Request must be enabled if the V385 is to set an interrupt when DOAC (Data Out Accepted) becomes true. Both registers will return a data code of one.

Clear/Disable INT Status (OFFSET 52_{16})

A read of this register will clear both the Read and the Write interrupt status bits. Also interrupts are disabled and the DIAC and DOPR input signals are set true. This register will always return a data code of one.

Clear Read INT Status (OFFSET $5A_{16}$)

A read of this register will clear the Read DIAC (Data In Accepted) interrupt status bit. This register will always return a data code of one.

Clear Write INT Status (OFFSET $5E_{16}$)

A read of this register will clear the Write DOPR (Data Output Present) interrupt status bit. This register will always return a data code of one.

Test Read INT Request (OFFSET 62_{16})
Test Write INT Request (OFFSET 66_{16})

These two registers are used to indicate which interrupt request is true. By reading either register a data code of one will indicate that either the Read or the Write request is true. A data code of zero will indicate that no request is pending. To test the Read INT request read the register at offset 62_{16}, and read the register at offset 66_{16} to test the Write INT request.

Test DP Status (OFFSET $6A_{16}$)
Test TC Status (OFFSET $6E_{16}$)

In a polling environment, these two registers are used to test the input status lines. Register $6A_{16}$ is used to determine if stable data is present at the input (DP = data present) and data has not been read. When this is the case a data code of one is returned. Register $6E_{16}$ is used to determine if the peripheral device is ready for a new word (TC = transfer complete). If this is the case then a data code of one is returned.

Test Status Input Bit (OFFSET 72_{16})

This register monitors a single status bit. This has general purpose use. For example, it may indicate if a peripheral is in the ON or OFF state. This low-true signal can be HTL or TTL by

module order option. If the input is LOW while reading this register, a data code of one will be returned.

DATA TRANFER OPERATIONS

Input Transfer Timing (Handshake Signals Used)

Two high-true handshake signals are provided for input data. Data Input present (DIPR) is set high by the external device, indicating that new data is present on the Data Input (DI) lines. When the data is read from the register at offset 12_{16}, the V385 asserts Data Input Accepted (DIAC), indicating that it has accepted the data and is ready for another data word.

For the following timing description refer to Figure 3 (see below). At time t_0 the peripheral device generates a "Data In" word, indicating this by setting DIPR to a high state. At time t_1 the V385 module detects DIPR set to a high state. (Due to high impedance pull-up resistors and low impedance open-collector drivers, the rise time of a signal will be longer than the fall time. DIPR and all other timing signals match the worst case when they are high-true). At time t_2, after a delay of 10 us (typical) for skew compensation, the Read interrupt source (ISR) and Data Present (DPR) become a Logic "1", indicating that the data is established.

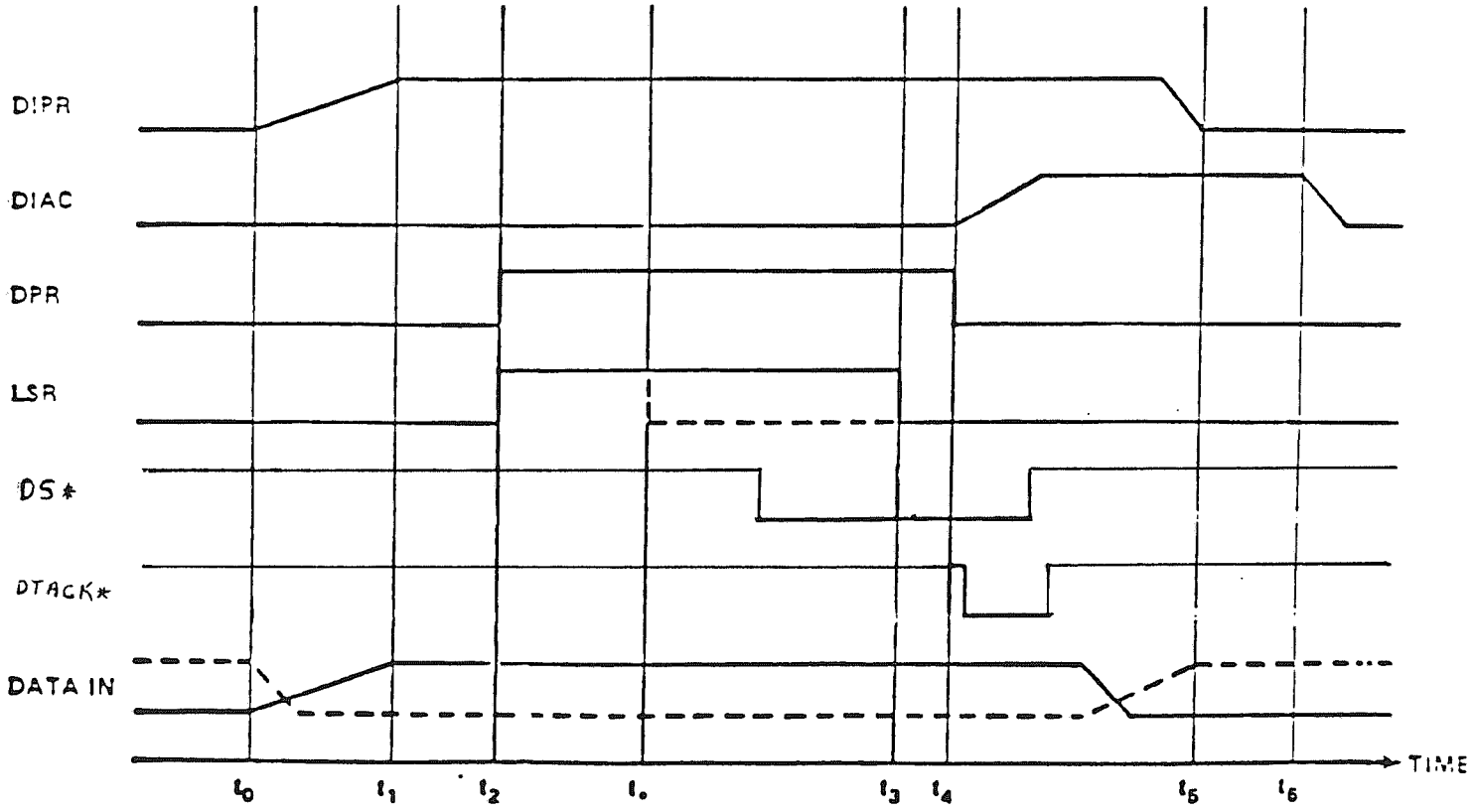


FIGURE 3 - V385 INPUT TIMING

At time t_3 the data is read by reading the register at offset 12_{16} which will also clear the Read interrupt status bit. (The Read interrupt status may be cleared earlier at time t. by reading register Clear Read INT Status offset $5A_{16}$). At time t_4 DIAC is set to a high state, indicating that the data has been read and may change. The DPR becomes a Logic "0".

When the peripheral device detects DIAC at a high state, it may change the data and set DIPR to a low state.

At time t_5, the v385 module receives DIPR in a low state and sets DIAC to a low state after a delay of 15 us (typical) at time t_6. Then the next transfer cycle may be started by the peripheral device.

Output Transfer Timing (Handshake Signals Used)

Two high-true handshake signals are provided for the output data. Data Output Present (DOPR) is set high by the V385 module, indicating that a new data word has been established by writing to the Output register. The peripheral device then sets DATA Output Accepted (DOAC) high to indicate that it has accepted the data and is ready for another data word. Note that only one pair of output handshake signals are available; for byte and nibble addressing, the handshake signals are not generally used.

For the following timing description refer to Figure 4 (see below). At time t_0 the V385 module receives DOAC in a low state, indicating that the preceding write cycle has been completed. The Write interrupt source (INT_SRC_W) and Transfer Complete (TC) signals become a Logic "1", indicating that the next data word can be transferred.

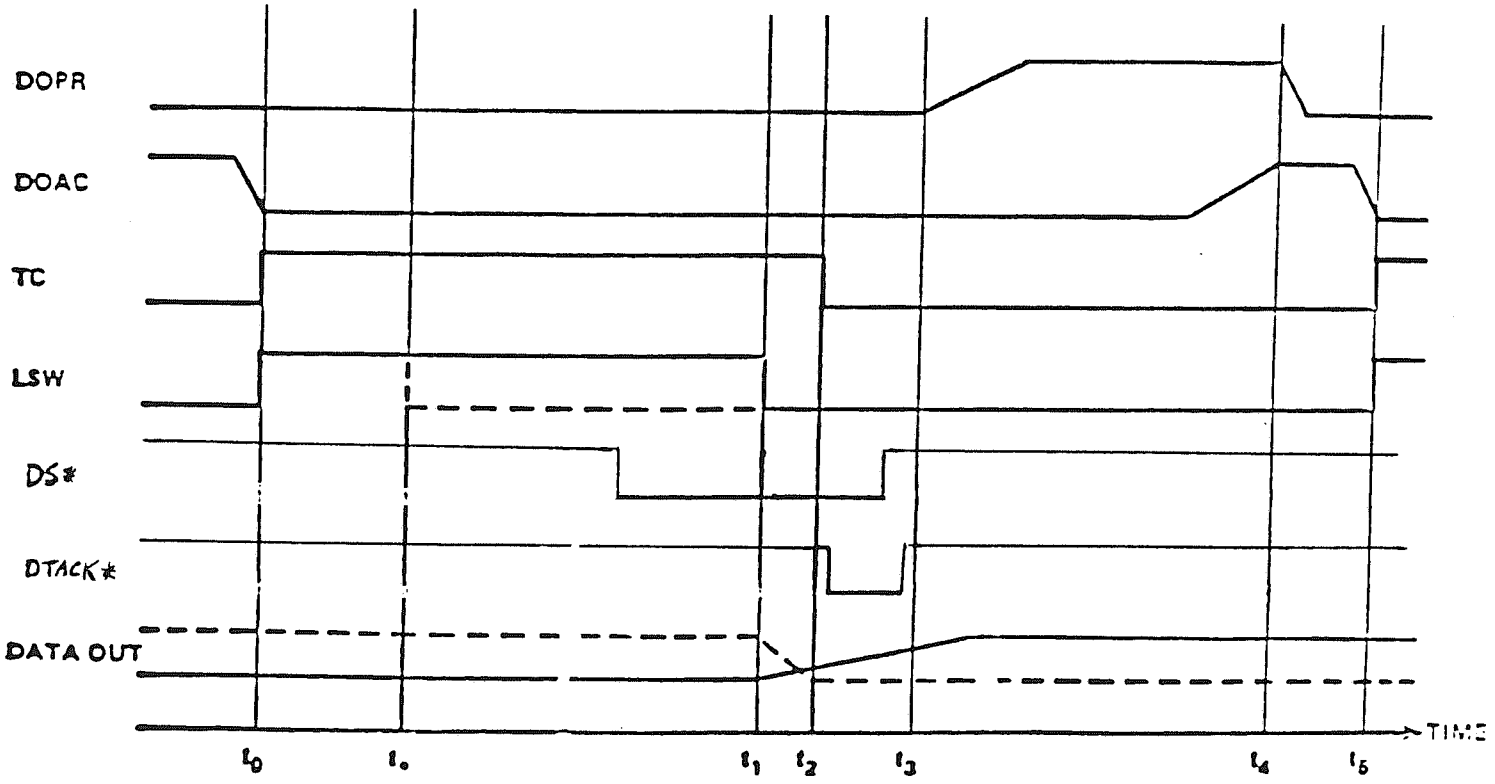


FIGURE 4 - V385 OUTPUT TIMING

At time t_1 the data word is written into the V385 module by writing to the Output register. This will clear the Write interrupt status bit. (The Write interrupt status may be cleared earlier at time t. by reading register Clear Write INT Status at offset $5E_{16}$). The status of the Data Out lines start to change. At time t_2 the TC signal becomes a Logic '0', and at time t_3, after a delay of 10 us (typical) for skew compensation, DOPR is set to a high state, indicating to the peripheral device that a new data word has been established. Having received DOPR in a high state, the peripheral device starts to accept the established data word and responds by setting DOAC to a high state.

At time t_4 the V385 module receives DOAC in a high state and sets DOPR to a low state but keeps the data word established until it receives DOAC in a low state.

DOAC goes to a low state and is detected at time t_5, the transfer cycle is completed, and a new data word may be established.

HTL or TTL Input Signal Standards

For the HTL option, all data inputs are low-true with logic "1" equal to a zero-to-six volts level, and logic "0" equal to a eight-to-15 volts. The two handshake signals that serve as inputs to the module have Schmitt trigger action with logic "0" equal to zero to 3.5 volts and logic "1" equal to 11 to 15 volts. The hysteresis level is set to about 3.5 volts. Each input has a 10 kohm pull-up to +15 volts.

For TTL option, all data inputs are low-true with logic "1" equal to zero to 0.6 volts and logic "0" equal to two to five volts. The two Schmitt trigger handshake signals that serve as inputs to the module have logic level of the following: logic "0" equal zero to 0.6 volts and logic "1" equals two to five volts, with a minimum hysterisis of 0.4 volts. Each input has a 10K ohm pull-up to +5 volts.

HTL or TTL Output Signal Standards

For the HTL option, the data output and handshake OUT signals are open collector and are diode-clamped to +15 volts. They have a drive capability of 30 mA maximum.

For the TTL option, the data output and handshake OUT signals are open-collector and contain internal 4076 ohm pull-up resistors to +5 volts.

POWER FOR REMOTE DEVICES

A +24 volt output is provided on the connector to power relays, etc. for the control outputs. This source is fused at 0.5 amp.

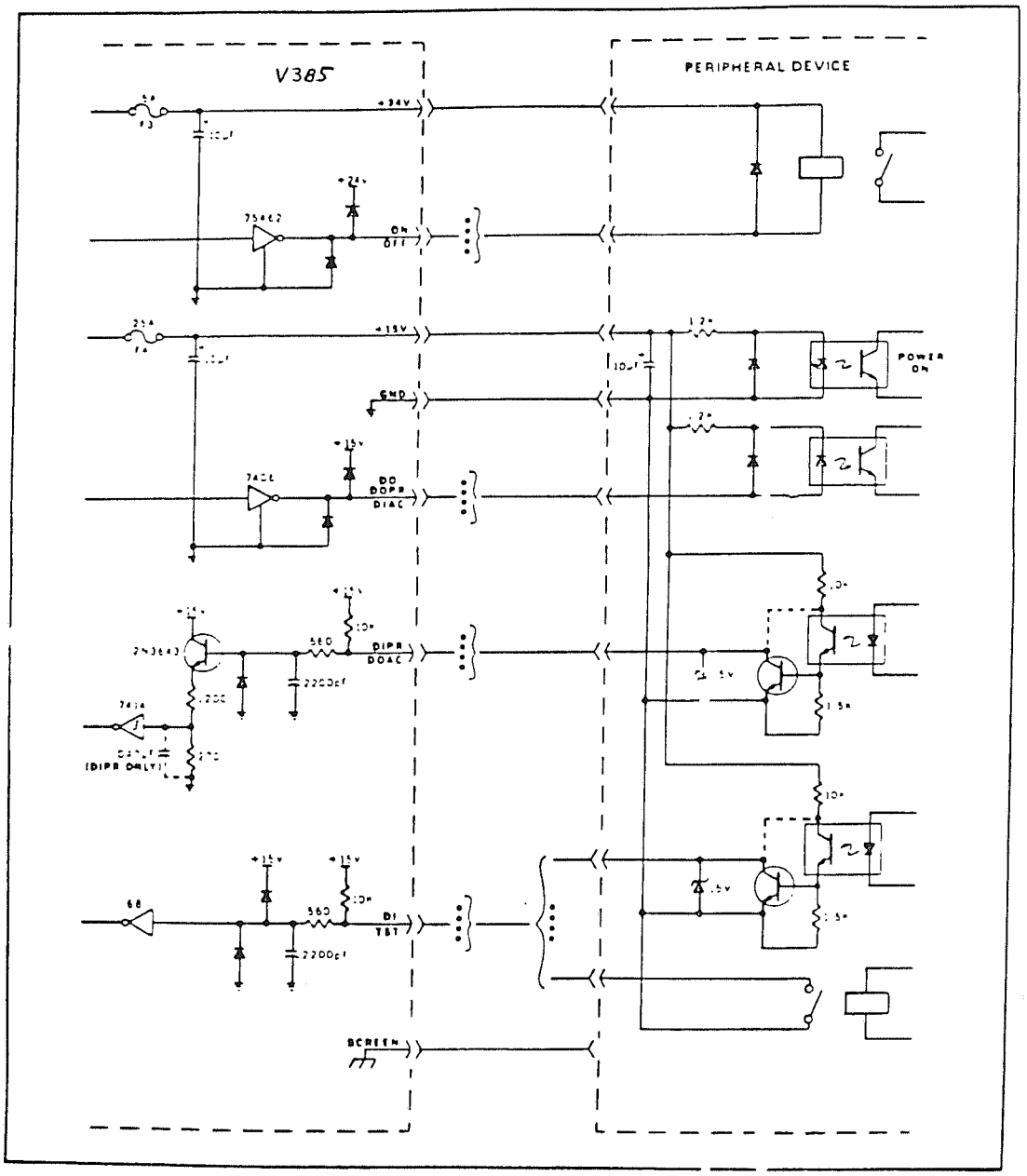
A +15 volt output is provided on the connector to power optically isolated interfaces, etc. in the peripheral device. This source is fused at 0.25 amp (+5 volts fused at 1 amp).

POWER-UP INITIALIZE

Power-up, SYSRESET*, or a read from the register at offset 52_{16} will clear all write data, disable interrupt requests, and stop the control pulse generation. In addition, DIAC will be set to high state; thus a read transfer from the peripheral device may be completed, and DOPR will be set to a high state. This starts a write transfer to the peripheral device and data will equal zero.

During power-up, DIAC and DOPR are set to a high state and are maintained for the duration of 500 milliseconds (typical) regardless of the state of DIPR and DOAC. Within that time, the handshake feature in the peripheral device must be set to a state with DIPR at a low state and DOAC at high state (unless the timing signals are not used).

OPTICAL ISOLATION INTERFACE, HTL OPTION



INTERRUPTS

The V385 can generate an interrupt from one of two sources. One from the Input register and the other from the Output register. The Input register will set an interrupt when a new data word is present and the Output register will set an interrupt when the peripheral device has accepted the output data.

The V385 must be set properly to interrupt the VXIbus. First, the interrupt switches must select one of seven Interrupt Requests by switching the appropriate IRQ switch to the "ON" position. Refer to the Interrupt Request Switch Selection for further information. Next, enable interrupts in the following manner:

Enable the Interrupt Request by reading the ENA Read/Write INT Request registers at offsets 42_{16} or $4A_{16}$.

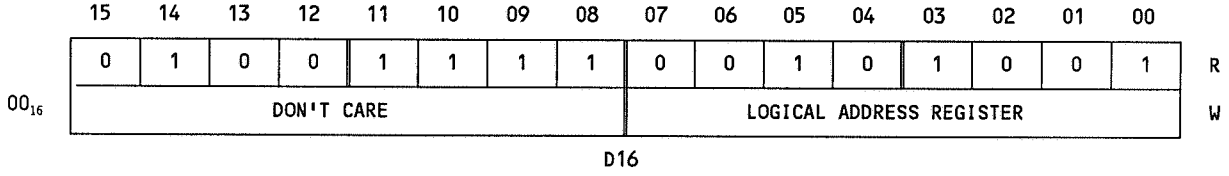
Enable Interrupts to the VXIBUS by writing Bit 4 in the Diagnostic Register with a Logical "1".

The V385 is now able to cause an interrupt on the VXIbus. Once the V385 sets an interrupt, an interrupt handler must read the Status/ID Register and reset the Enable Interrupt bit in the Diagnostic Register to a Logical "0". At this time, the interrupt request should be cleared which will also clear INT SRC in the Diagnostic Register to a Logical "0". To clear an Interrupt request, read the Test Read/Write INT Request Registers at offsets 62_{16} or 66_{16} to determine which interrupt status bit is causing the interrupt. Then clear the interrupt status bit with the appropriate clear function. Refer to Table 2, V385 Operational Register, for a list of clear functions. Once INT SRC Bit 3 in the Diagnostic Register is set to a Logical "0", the Interrupt Enable Bit 4 in the Diagnostic Register can be set to a Logical "1". If INT SRC is a Logical "1" when INT ENA is set to a Logical "1", an interrupt will occur instantly.

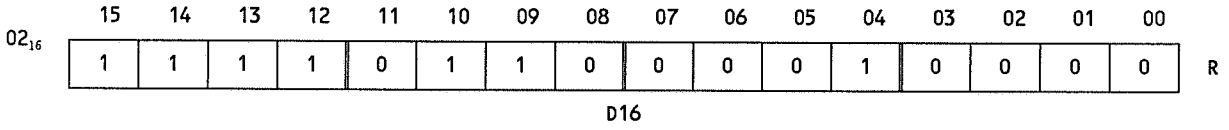
V385 REGISTER LAYOUT

CONFIGURATION REGISTERS

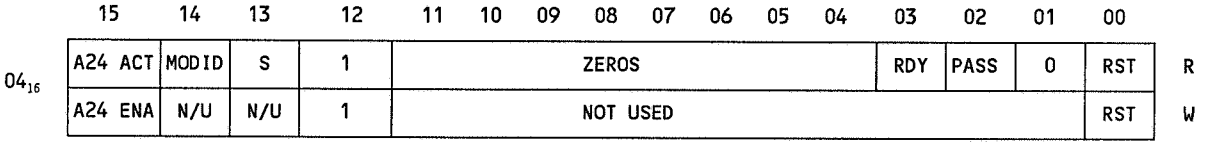
ID/Logical Address Register



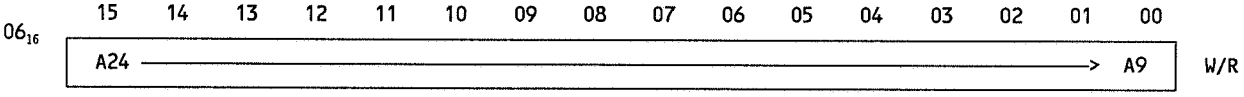
Device Type



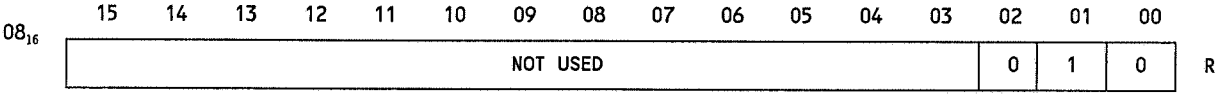
Status/Control Register



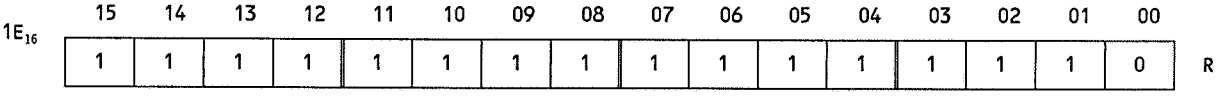
Offset Register



Attribute Register



Subclass Register



OPERATIONAL REGISTERS

Diagnostic Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care								D	S	0	INT ENA	INT SRC	0	0	0	R
00_{16}	Don't Care								0	0	0	INT ENA	0	0	CLR	INIT	W

Interrupt Status/ID Register 02

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	STATUS								ID								R

INPUT REGISTER

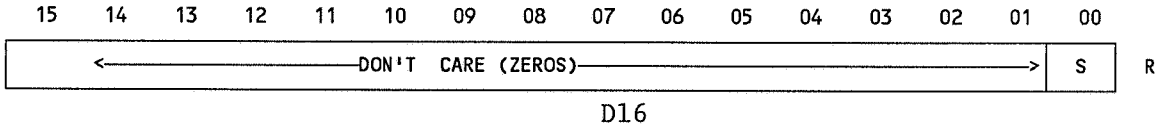
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
12_{16}	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R

OUTPUT REGISTERS

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
16_{16}	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W
$1A_{16}$	DON'T CARE								W8	W7	W6	W5	W4	W3	W2	W1	W
$1E_{16}$	W16	W15	W14	W13	W12	W11	W10	W9	DON'T CARE								W
22_{16}	DON'T CARE												W4	W3	W2	W1	W
26_{16}	DON'T CARE								W8	W7	W6	W5	DON'T CARE				W
$2A_{16}$	DON'T CARE				W12	W11	W10	W9	DON'T CARE								W
$2E_{16}$	W16	W15	W14	W13	DON'T CARE												W

OPERATIONAL CONTROL REGISTERS

32_{16}	Execute Pulse A
36_{16}	Execute Pulse B
$3A_{16}$	Execute Pulse C
$3E_{16}$	Execute Pulse D
42_{16}	Enable Read INT Request
46_{16}	Disable Read INT Request
$4A_{16}$	Enable Write INT Request
$4E_{16}$	Disable Write INT Request
52_{16}	Clear/Disable INT Status
56_{16}	Reserved
$5A_{16}$	Clear Read INT Status
$5E_{16}$	Clear Write INT Status
62_{16}	Test Read INT Request
66_{16}	Test Write INT Request
$6A_{16}$	Test DP Status
$6E_{16}$	Test TC Status
72_{16}	Test Status Input Bit



D16

WARRANTY

KineticSystems Company, LLC warrants its standard hardware products to be free of defects in workmanship and materials for a period of one year from the date of shipment to the original end user. Software products manufactured by KineticSystems are warranted to conform to the Software Product Description (SPD) applicable at the time of purchase for a period of ninety days from the date of shipment to the original end user. Products purchased for resale by KineticSystems carry the original equipment manufacturer's warranty.

KineticSystems will, at its option, either repair or replace products that prove to be defective in materials or workmanship during the warranty period.

Transportation charges for shipping products to KineticSystems shall be prepaid by the purchaser, while charges for returning the repaired warranty product to the purchaser, if located in the United States, shall be paid by KineticSystems. Return shipment will be made by UPS, where available, unless the purchaser requests a premium method of shipment at their expense. The selected carrier shall not be construed to be the agent of KineticSystems, nor will KineticSystems assume any liability in connection with the services provided by the carrier.

The product warranty may vary outside the United States and does not include shipping, customs clearance, or any other charges. Consult your local authorized representative or reseller for more information regarding specific warranty coverage and shipping details.

PRODUCT SPECIFICATIONS AND DESCRIPTIONS IN THIS DOCUMENT SUBJECT TO CHANGE WITHOUT NOTICE.

KINETICSYSTEMS SPECIFICALLY MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR ANY OTHER WARRANTY EITHER EXPRESSED OR IMPLIED, EXCEPT AS IS EXPRESSLY SET FORTH HEREIN. PRODUCT FAILURES CREATED BY UNAUTHORIZED MODIFICATIONS, PRODUCT MISUSE, OR IMPROPER INSTALLATION ARE NOT COVERED BY THIS WARRANTY.

THE WARRANTIES PROVIIDED HEREIN ARE THE PURCHASER'S SOLE AND EXCLUSIVE REMEDIES ON ANY CLAIM OF ANY KIND FOR ANY LOSS OR DAMAGE ARISING OUT OF, CONNECTED WITH, OR RESULTING FROM THE USE, PERFORMANCE OR BREACH THEREOF, OR FROM THE DESIGN, MANUFACTURE, SALE, DELIVERY, RESALE, OR REPAIR OR USE OF ANY PRODUCTS COVERED OR FURNISHED BY KINETICSYSTEMS INCLUDING BUT NOT LIMITED TO ANY CLAIM OF NEGLIGENCE OR OTHER TORTIOUS BREACH, SHALL BE THE REPAIR OR REPLACEMENT, FOB FACTORY, AS KINETICSYSTEMS MAY ELECT, OF THE PRODUCT OR PART THEREOF GIVING RISE TO SUCH CLAIM, EXCEPT THAT KINETICSYSTEMS' LIABILITY FOR SUCH REPAIR OR REPLACEMENT SHALL IN NO EVENT EXCEED THE CONTRACT PRICE ALLOCABLE TO THE PRODUCTS OR PART THEROF WHICH GIVES RISE TO THE CLAIM. IN NO EVENT SHALL KINETICSYSTEMS BE LIABLE FOR DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING LOSS OF PROFITS.

Products will not be accepted for credit or exchange without the prior written approval of KineticSystems. If it is necessary to return a product for repair, replacement or exchange, a Return Authorization (RA) Number must first be obtained from the Repair Service Center prior to shipping the product to KineticSystems. The following steps should be taken before returning any product:

1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com