Model V500

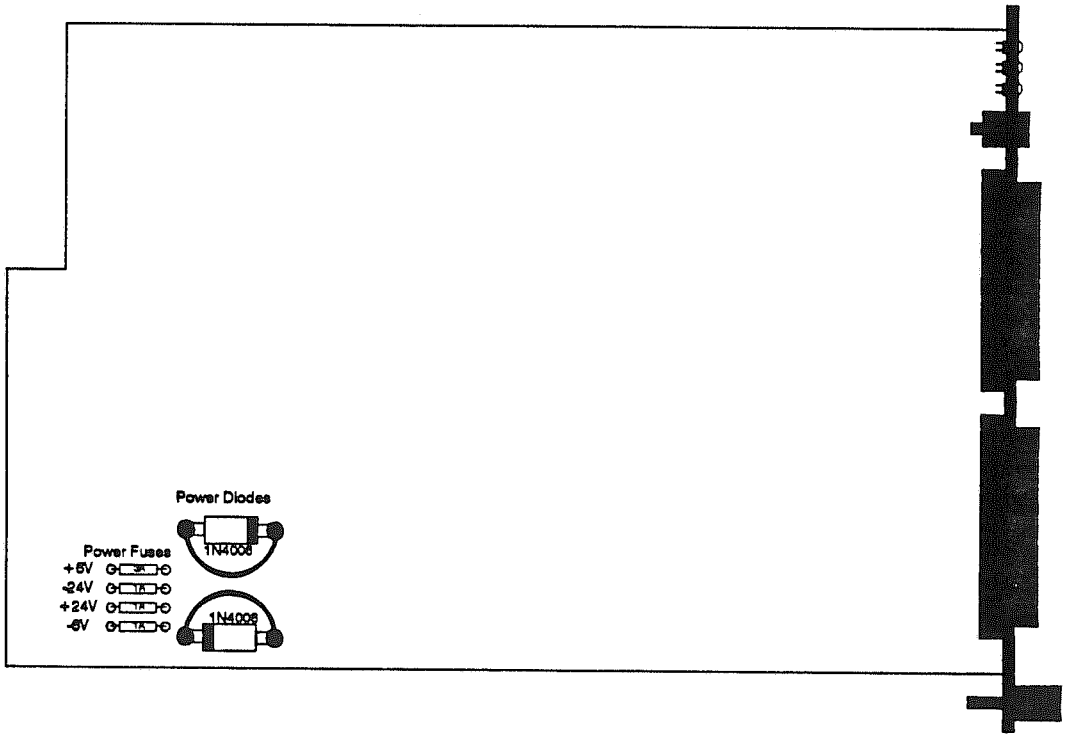
CAMAC-to-VXI*bus* Adaptor

INSTRUCTION MANUAL

June, 1993

* * * WARNING * * *

Because of the voltage requirements of a CAMAC crate, a shorting strap must be placed across the +6 Volt and the -6 Volt diodes on the CAMAC module. (See drawing below.)



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Warranty
PTS:rem

CAMAC-to-VXIbus Adapter

Use CAMAC (IEEE-583) modules in a VXI mainframe

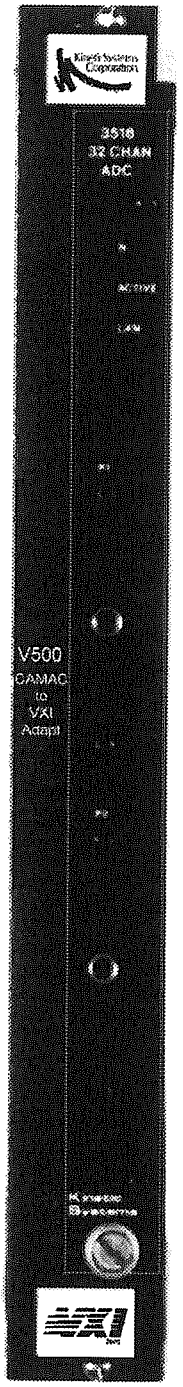
V500

Features

- **Brings CAMAC functionality to VXIbus platforms**
- **Preserves CAMAC instrumentation investment**
- **Accommodates single-wide CAMAC modules**
- **Maps CAMAC function code/subaddress combinations to VME/VXI address space**
- **Complies with IEEE Standards 583 (CAMAC) and 1155 (VXIbus)**

Typical Applications

- **High energy physics experiments**
- **Nuclear accelerator control and monitoring**
- **General-purpose testing**



V500 shown with 3516 CAMAC ADC module

General Description (Product specifications and descriptions subject to change without notice.)

The KineticSystems Model V500 is a single-width, C-size, register-based, VXIbus module that allows you to add I/O functionality presently found in CAMAC instrumentation to a VXIbus environment. It is ideally suited to situations where a CAMAC module is the only format in which a particular function is available. Likewise, at organizations which have large investments in CAMAC-based instrumentation but (because of changes in control and/or data acquisition philosophies and architectures) are implementing new systems in VXIbus, the V500 provides a convenient means of "recycling" that instrumentation.

The V500 is an adapter that accepts a wide variety of CAMAC modules. An 86-position printed circuit edge connector receives the CAMAC module's Dataway contacts, and a tapped block attached to the V500's front panel mounting hardware accepts the CAMAC module's jack-screw. Fuses are provided on the adapter for the six power lines tied to the Dataway connector's power pins (±24, ±12, +5 and -5.2 V). Because of differences between the CAMAC and VXIbus specifications, the dropping diodes or transistors normally found on the CAMAC module's ±6 V power lines must be bypassed (shorted from input to output) prior to use in the V500.

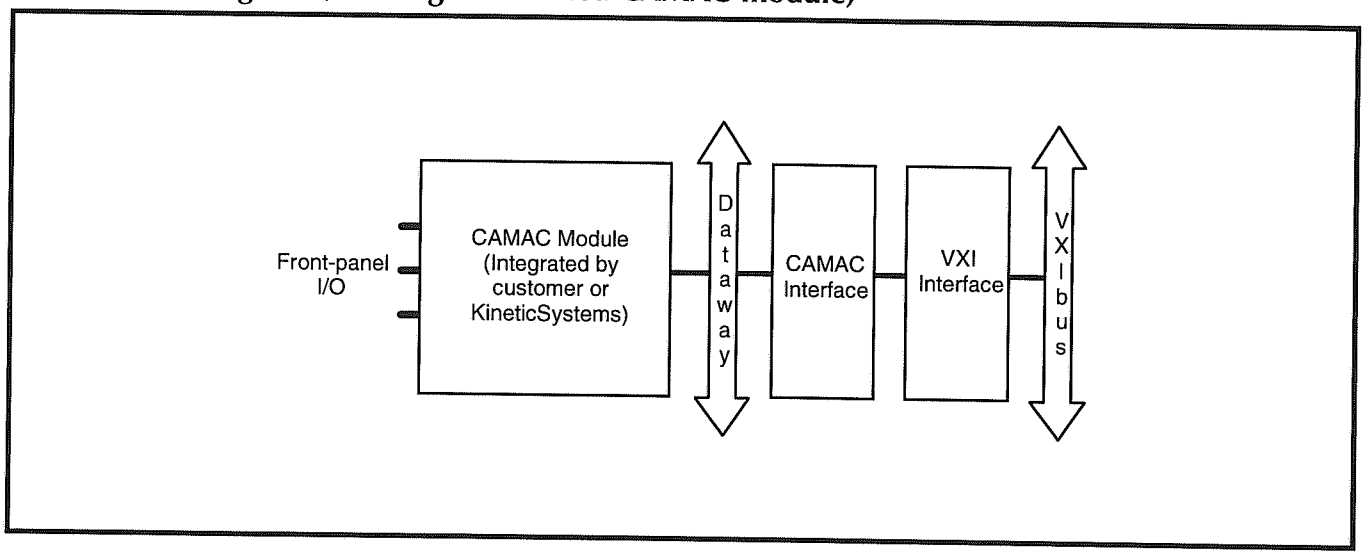
In a VXIbus system, the V500 (and the CAMAC module mounted within) looks like an extended, register-based device. A fully standardized VXIbus interface is present on the module. The Offset Register in the defined Configuration Register area points to an area in the standard (A24) address space where the CAMAC functions can be accessed. A PROM-based circuit converts access to the addresses into a CAMAC "Dataway cycle" with a particular CAMAC Function Code and Subaddress combination asserted. All Function Code/Subaddress combinations are possible. The Q and X responses from each CAMAC cycle are captured in a status register. This register can be interrogated at any time to determine the state of Q and X for the last cycle executed.

In its standard form, the V500 anticipates that the CAMAC module's I/O connections will be completed through plugs or receptacles mounted to that module's front panel. For modules whose I/O connections are normally accomplished at the rear of the module (i.e., at connectors mounted in the "free space" above the Dataway connector), contact KineticSystems for advice and assistance.

The V500 is available with or without integration services. The basic unit is provided with enough documentation so that you can mount your own CAMAC module. The documentation describes register layouts and access procedures as an aid in software development. Optionally, you may send us a CAMAC module for integration. The module may be one of KineticSystems' manufacture or one manufactured elsewhere. Integration consists of mounting the module in the adapter and executing a basic response test. A computer generated printout of the Q and X responses from this test will be returned as part of this program. For greater levels of integration, functional testing, and software development assistance, consult the factory.

The V500 supports both static and dynamic configuration. It may be accessed using A24/A16, D16 data transfers.

V500 Block Diagram (showing an inserted CAMAC module)



Item	Specification
CAMAC Module Size	One single-width unit, as per IEEE Standard 583 (305 mm x 182.9 mm x 17 mm)
Cycle Time at CAMAC Module	1 µs
Power Available to CAMAC Module	
+5 V	5 A
-5.2 V	5 A
±12 V	2 A, each line
±24 V	2 A, each line
Environmental and Mechanical (VXI)	
Operating temperature	0°C to +50°C
Storage temperature	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V500-ZA11 Single-width CAMAC-to-VXIbus Adapter

Model V500-1000 Integration Service.

Notes: The V500-ZA11 Adapter includes adapter, mapping PROM and documentation.

The V500-1000 Integration Service consists of mounting a user-supplied CAMAC module within a V500 Adapter (purchased separately), CAMAC response testing, and a test printout.

Related Products

A single-width CAMAC module (produced by KineticSystems or another manufacturer)

UNPACKING AND INSTALLATION

The Model V500 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V500 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device.) The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V500 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating the eight rocker switches located under the access hole in the module's right side ground shield. Refer to FIGURE 1.

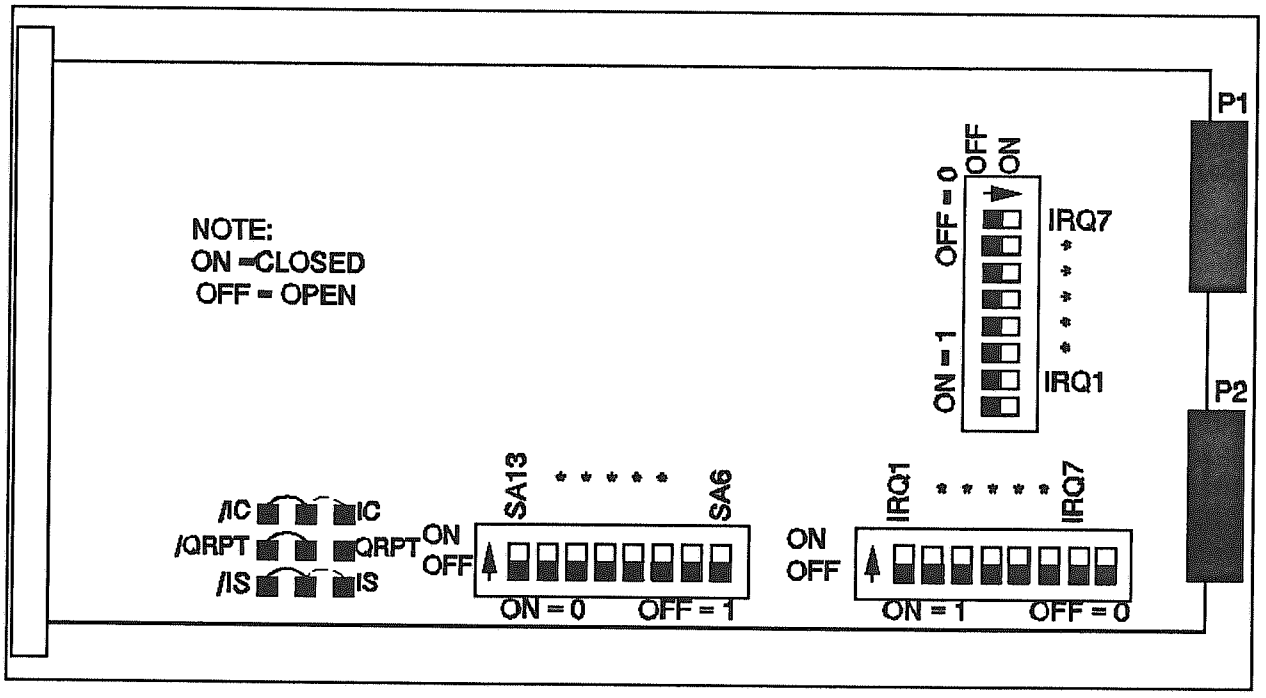


FIGURE 1 - V500 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from 0 to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value. Closing a switch sets its corresponding bit to a "0", opening a switch sets its bit to a "1".

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	LA128	LA64	LA32	LA16	LA08	LA04	LA02	LA01	0	0	0	0	0	0

Bits 15 and 14 are set to "1" (**VXI** defined).

Bits 13 through 6 are user-selectable via the address switches LA128-LA1.

Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches and Straps

The V500 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to **FIGURE 1** for the switch locations and settings. Both banks of switches must be set to the same value.

The V500 has two straps which are used to enable or disable the V500's ability to process interrupts.

The strap labeled IC is used to enable or disable the V500's Interrupt Handler Control capability. This strap is directly tied to the V500's Attribute Register bit 2 position. With the strap in the IC position, the V500 Attribute Register bit 2 will be read as a "0", indicating that the Interrupt Handler Control option is implemented. With the strap in the /IC position, the V500's Attribute Register bit 2 will be read as a "1", indicating that the Interrupt Handler Control option is not implemented.

The strap labeled IS is used to enable or disable the V500's Interrupt Status reporting capability. This strap is directly tied to the V500's Attribute Register bit 0 position. With the strap in the IS position, the V500 Attribute Register bit 2 will be read as a "0", indicating that the Interrupt Status reporting option is implemented. With the strap in the /Is position, the V500's Attribute Register bit 2 will be read as a "1", indicating that the Interrupt Status reporting option is not implemented.

Interrupt Handler Control and Status reporting are used to process CAMAC LAMS from the CAMAC module inserted into the V500.

CAMAC Module Insertion

Select the various strap and switch settings of the V500 and the CAMAC module (for configuration of the CAMAC module, refer to the Operating Manual of the CAMAC module for configuring the various options of the module).

Because of the voltage requirements of a CAMAC crate, a shorting strap must be placed across the +6 Volt and the -6 Volt diodes on the CAMAC module. (See FIGURE 2 on page 27.)

Place the CAMAC module into the edge connector on the V500. The component side of the module will face the V500 mother board. Secure the CAMAC module to the V500 by tightening the CAMAC module jack screw.

V500 Module Insertion

The V500 is a C-sized single-width VXIbus module. Except for Slot 0, it can be mounted in any unoccupied slot in a C-sized VXI mainframe.

CAUTION:	**TURN THE MAINFRAME POWER OFF PRIOR TO INSERTING OR REMOVING THE MODULE.**

WARNING:	**REMEMBER TO REMOVE THE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE INTO THE BACKPLANE.**

To insure proper interrupt acknowledge cycles from the V500 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Daisy-chain jumpers must be in any empty slot between the V500 and Slot 0 Controller.

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration registers, the V500 implements those required for register-based devices. The V500 also contains a set of Operational Registers to monitor and control the functional aspects of the device. Both sets of registers are described in this section.

VXIbus Configuration Registers

Configuration registers are required by the VXIbus specification so that appropriate levels of system configuration can be accomplished. Access to the Configuration registers for all VXIbus modules is available through the VMEbus short (A16) address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

The Configuration registers in the V500 are offset from the base address. **Note: The V500 only responds to these addresses if the Short Nonprivileged Access (29_{16}) or Short**

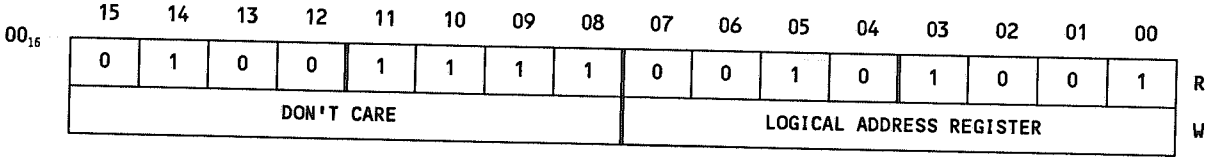
Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle. TABLE 1 shows the applicable Configuration Registers present in the V500, their offset from the base (Logical) address, and their Read/Write capabilities.

TABLE I
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET (HEX)	W/R MODE	REGISTER NAME
00_{16}	W/R	ID/Logical Address Register
02_{16}	R	Device Type Register
04_{16}	W/R	Status/Control Register
06_{16}	W/R	Offset Register
08_{16}	R	Attribute Register
$1E_{16}$	R	Subclass Register

ID/Logical Address Register

The format and bit assignments for the ID/Logical Address Register are as follows



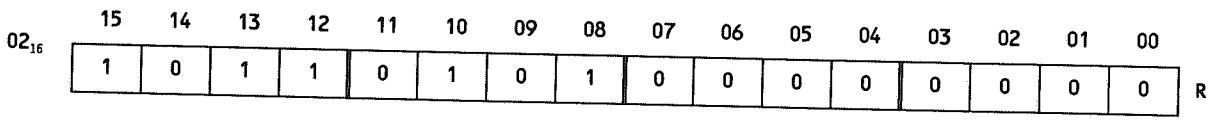
On Read transactions:

Bit(s)	Mnemonics	Meaning
15, 14	Device Class	This is a Register-Based Device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For Write transactions, bits 15 through 8 are not used, and writing them has no effect on the V500. In Dynamically configured systems (i.e., the Logical Address switches are set to a value of 255), bits 7 through 0 are written with the new Logical Address value.

Device Type Register

The format for the Device Type Register is as follows:



On Read transactions:

Bit(s)	Mnemonics	Meaning
15 - 12	Required Memory	The V500 requires 4096 bytes of additional memory space.
11 - 00	Model Code	Identifies this module as Model V500 (500_{16}).

Status/Control Register

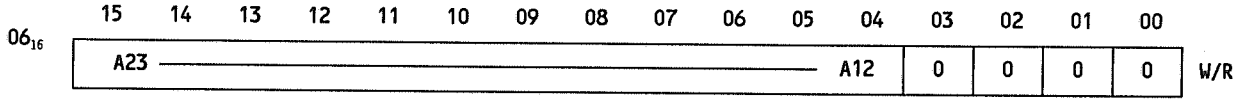
04_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
A24	MODID	S	1	ZEROS								RDY	PASS	N/U	RST	R
A24	N/U	N/U	1	NOT USED											RST	W

Bit(s)	Mnemonics	Meaning
15	A24	Writing a "1" to this bit will enable A24 addressing and allow access to the V500's Operational Registers. Reading a "1" indicates that A24 addressing is active. This bit is reset to a "0" on power-up or the assertion of STSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on the VXIBus P2 connector. A "0" will indicate that the device is selected by a high state on the P2 MODID line.
13	STATUS	This Read-Only bit indicates the status of the last transaction to one of the V500's operational registers. A "1" indicates that the transaction was completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written as a "1".
11 - 4	NOT USED	These bits are not used and are read as "0".
3	RDY	READY. The V500 is always "ready". This bit is read as a "1".

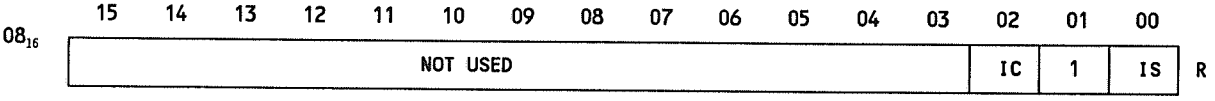
2	PASS	The V500 will always pass it's self tests. This bit is read as a "1".
1	N/U	This bit is not used and is read as a "0".
0	RST	RESET. This Read/Write bit controls the Soft Reset condition within the V500. While the Soft Reset condition is enabled (by writing a "1" to this bit), any further access to the Operational registers, except for the Diagnostic and Interrupt Status Registers, is inhibited. The output bit patterns from the module are maintained in the state they were just prior to the Soft Reset being enabled. This bit can be cleared by writing a "0" to this bit location, on power-up, or by the assertion of SYSRESET*.

Offset Register



This 16 bit Read/Write register defines the base address of the A24 Operational Registers. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Attribute Register



Bit(s)	Mnemonics	Meaning
15 - 03	NOT USED	These bits are not used and are read as zeros.
02	IC	When read as "0", this bit indicates that the V500 has Interrupt Control capabilities.
01	1	This bit indicates that the V500 does not have interrupt Handler capabilities.
00	IS	When read as "0", this bit indicates that the V500 has an Interrupt Status Register.

Subclass Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	R

The Subclass Register defines the V500 as a VXIbus Extended Device.

OPERATIONAL REGISTERS

The Operational Registers are the method of accessing the functional registers of the V500 and the CAMAC module. These registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 bit (bit 15) must be set in the Status/Control Register. **Note: The V500 will only respond to these addresses if the Standard Nonprivileged Data Access (39_{16}), Standard Nonprivileged Program Access ($3A_{16}$), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for the bus cycle(s).**

TABLE 2 shows the applicable Operational Registers present in the V500, their offset from the base, and their Read/Write capabilities.

TABLE 2
V500 OPERATIONAL REGISTERS - STANDARD ADDRESS (A24) SPACE

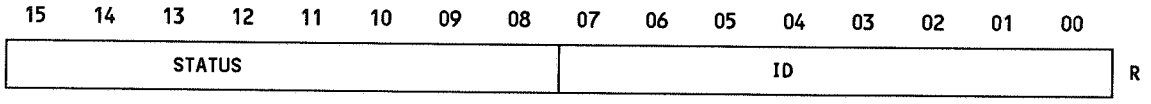
A24 OFFSET	W/R MODE	REGISTER NAME
00_{16}	W/R	Diagnostic Register
02_{16}	R	Interrupt Status Register
802_{16}-$9FF_{16}$	R	CAMAC read command register
$A02_{16}$-BFF_{16}	R	CAMAC F(8) through F(15) register
$C02_{16}$-DFF_{16}	W	CAMAC write command registers
$E02_{16}$-FFF_{16}	R	CAMAC F(24) through F(31) registers

Diagnostic Register 00_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
NOT USED								X	Q	N/U	IE	IS	N/U	N/U	N/U	R
NOT USED								0	0	0	IE	0	I	CLR	INIT	W

Bit(s)	Mnemonics	Meaning
15 - 08	NOT USED	These bits are not used and are read as "0".
07	X	When set to a "1", this read only bit indicates that the last register access to a CAMAC Operational Registers (offset 800_{16} through FFF_{16}) was valid and that the CAMAC module responded with a CAMAC X = 1.
06	Q	When set to a "1", this read only bit indicates that the last register access to a CAMAC Operational Registers (offset 800_{16} through FFF_{16}) was accepted and that the CAMAC module responded with a CAMAC Q = 1.
05	N/U	This bit is not set and is read as "0".
04	IE	Setting this bit to a "1" will enable the CAMAC LAM response to set a VXIbus interrupt.
03	IS	When set, this read only bit indicates that the CAMAC module has asserted its LAM bit on the CAMAC connector L line.
02	I	Setting this bit to a "1" will cause the CAMAC Inhibit line to be asserted.
01	CLR	Setting this bit to a "1" will clear the CAMAC Operational Registers (800_{16} through FFF_{16}). Setting this bit causes the V500 to execute a CAMAC C cycle to the CAMAC module. The Diagnostic Registers are unaffected.
00	INIT	Setting this bit to a "1" will only reset the CAMAC Operational Register (800_{16} through FFF_{16}). Setting this bit causes the V500 to execute a CAMAC Z cycle to the CAMAC module. The Diagnostic Registers are unaffected.

Interrupt Status/ID Register 02_{16}



During an interrupt acknowledge cycle, this Read-only register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16 bits will be pulled to a logic "1" by the backplane termination networks.

Bit(s)	Mnemonics	Meaning
15 - 08	STATUS	These eight bits will indicate Request True or Request False. Request True = FD_{16} Request False = FC_{16}
07 - 00	ID	These bits represent the Logical Address of the V500 Configuration Register.

CAMAC Operational Registers

The CAMAC Operational Registers are used to access functions on the CAMAC card which is inserted in the V500 CAMAC connector. These registers are mapped in A24 address space and begin at offset 800_{16}.

The CAMAC read and write data format is as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
offset	NOT USED								RW24	RW23	RW22	RW21	RW20	RW19	RW18	RW17
offset+2	RW16	RW15	RW14	RW13	RW12	RW11	RW10	RW09	RW08	RW07	RW06	RW05	RW04	RW03	RW02	RW01

The base address of the CAMAC register is a long word aligned offset of the V500 Logical Address beginning at 800_{16}. Individual CAMAC F and A functions are long word offsets of the A24 offset. For the description of the CAMAC register map, the term offset refers to the long word offset from the A24 base address.

During writes to the CAMAC module, the upper eight bits of CAMAC data (RW17 - RW24) are required to be written, then the Offset for the desired function must be written prior to writing the Offset + 2 address (RW01 - RW16) data value. The CAMAC cycle will be executed to the CAMAC module during the write of the Offset + 2 register. If only the lower sixteen bits of write data are required for the CAMAC operation, then a write to the Offset + 2 address is required.

To maintain compatibility with the CAMAC write functions, CAMAC read and CAMAC Control functions are performed to the Offset + 2 register address. The Offset + 2 address will contain the lower sixteen bits of CAMAC read data during read operations. The upper eight bits of CAMAC read data will be stored in the Offset register address. Upon a read of the Offset + 2 register, a CAMAC cycle will be preformed.

During CAMAC Control functions, the returned data codes in the Offset + 2 register reflect the state of the CAMAC Q response from the CAMAC module. A code of "1" indicates that the module returned a CAMAC Q. A code of "0" indicates that the module did not return a CAMAC Q. CAMAC Control functions must be performed as reads to the Offset + 2 address for the given command.

TABLE 3 is a list of the decoded CAMAC F and A commands, their A24 offset, and their Read/Write accessibility.

TABLE 3
V500 CAMAC FUNCTION CODE AND SUBADDRESS REGISTER DECODE

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
802	F(0)A(0)	R
806	F(0)A(1)	R
80A	F(0)A(2)	R
80E	F(0)A(3)	R
812	F(0)A(4)	R
816	F(0)A(5)	R
81A	F(0)A(6)	R
81E	F(0)A(7)	R
822	F(0)A(8)	R
826	F(0)A(9)	R
82A	F(0)A(10)	R
82E	F(0)A(11)	R
832	F(0)A(12)	R
836	F(0)A(13)	R
83A	F(0)A(14)	R
83E	F(0)A(15)	R
842	F(1)A(0)	R
846	F(1)A(1)	R
84A	F(1)A(2)	R
84E	F(1)A(3)	R
852	F(1)A(4)	R
856	F(1)A(5)	R
85A	F(1)A(6)	R
85E	F(1)A(7)	R
862	F(1)A(8)	R
866	F(1)A(9)	R
86A	F(1)A(10)	R
86E	F(1)A(11)	R
872	F(1)A(12)	R
876	F(1)A(13)	R
87A	F(1)A(14)	R

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
87E	F(1)A(15)	R
882	F(2)A(0)	R
886	F(2)A(1)	R
88A	F(2)A(2)	R
88E	F(2)A(3)	R
892	F(2)A(4)	R
896	F(2)A(5)	R
89A	F(2)A(6)	R
89E	F(2)A(7)	R
8A2	F(2)A(8)	R
8A6	F(2)A(9)	R
8AA	F(2)A(10)	R
8AE	F(2)A(11)	R
8B2	F(2)A(12)	R
8B6	F(2)A(13)	R
8BA	F(2)A(14)	R
8BE	F(2)A(15)	R
8C2	F(3)A(0)	R
8C6	F(3)A(1)	R
8CA	F(3)A(2)	R
8CE	F(3)A(3)	R
8D2	F(3)A(4)	R
8D6	F(3)A(5)	R
8DA	F(3)A(6)	R
8DE	F(3)A(7)	R
8E2	F(3)A(8)	R
8E6	F(3)A(9)	R
8EA	F(3)A(10)	R
8EE	F(3)A(11)	R
8F2	F(3)A(12)	R
8F6	F(3)A(13)	R
8FA	F(3)A(14)	R
8FE	F(3)A(15)	R
902	F(4)A(0)	R
906	F(4)A(1)	R

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
90A	F(4)A(2)	R
90E	F(4)A(3)	R
912	F(4)A(4)	R
916	F(4)A(5)	R
91A	F(4)A(6)	R
91E	F(4)A(7)	R
922	F(4)A(8)	R
926	F(4)A(9)	R
92A	F(4)A(10)	R
92E	F(4)A(11)	R
932	F(4)A(12)	R
936	F(4)A(13)	R
93A	F(4)A(14)	R
93E	F(4)A(15)	R
942	F(5)A(0)	R
946	F(5)A(1)	R
94A	F(5)A(2)	R
94E	F(5)A(3)	R
952	F(5)A(4)	R
956	F(5)A(5)	R
95A	F(5)A(6)	R
95E	F(5)A(7)	R
962	F(5)A(8)	R
966	F(5)A(9)	R
96A	F(5)A(10)	R
96E	F(5)A(11)	R
972	F(5)A(12)	R
976	F(5)A(13)	R
97A	F(5)A(14)	R
97E	F(5)A(15)	R
982	F(6)A(0)	R
986	F(6)A(1)	R
98A	F(6)A(2)	R
98E	F(6)A(3)	R
992	F(6)A(4)	R

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
996	F(6)A(5)	R
99A	F(6)A(6)	R
99E	F(6)A(7)	R
9A2	F(6)A(8)	R
9A6	F(6)A(9)	R
9AA	F(6)A(10)	R
9AE	F(6)A(11)	R
9B2	F(6)A(12)	R
9B6	F(6)A(13)	R
9BA	F(6)A(14)	R
9BE	F(6)A(15)	R
9C2	F(7)A(0)	R
9C6	F(7)A(1)	R
9CA	F(7)A(2)	R
9CE	F(7)A(3)	R
9D2	F(7)A(4)	R
9D6	F(7)A(5)	R
9DA	F(7)A(6)	R
9DE	F(7)A(7)	R
9E2	F(7)A(8)	R
9E6	F(7)A(9)	R
9EA	F(7)A(10)	R
9EE	F(7)A(11)	R
9F2	F(7)A(12)	R
9F6	F(7)A(13)	R
9FA	F(7)A(14)	R
9FE	F(7)A(15)	R
A02	F(8)A(0)	R
A06	F(8)A(1)	R
A0A	F(8)A(2)	R
A0E	F(8)A(3)	R
A12	F(8)A(4)	R
A16	F(8)A(5)	R
A1A	F(8)A(6)	R
A1E	F(8)A(7)	R

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
A22	F(8)A(8)	R
A26	F(8)A(9)	R
A2A	F(8)A(10)	R
A2E	F(8)A(11)	R
A32	F(8)A(12)	R
A36	F(8)A(13)	R
A3A	F(8)A(14)	R
A3E	F(8)A(15)	R
A42	F(9)A(0)	R
A46	F(9)A(1)	R
A4A	F(9)A(2)	R
A4E	F(9)A(3)	R
A52	F(9)A(4)	R
A56	F(9)A(5)	R
A5A	F(9)A(6)	R
A5E	F(9)A(7)	R
A62	F(9)A(8)	R
A66	F(9)A(9)	R
A6A	F(9)A(10)	R
A6E	F(9)A(11)	R
A72	F(9)A(12)	R
A76	F(9)A(13)	R
A7A	F(9)A(14)	R
A7E	F(9)A(15)	R
A82	F(10)A(0)	R
A86	F(10)A(1)	R
A8A	F(10)A(2)	R
A8E	F(10)A(3)	R
A92	F(10)A(4)	R
A96	F(10)A(5)	R
A9A	F(10)A(6)	R
A9E	F(10)A(7)	R
AA2	F(10)A(8)	R
AA6	F(10)A(9)	R
AAA	F(10)A(10)	R

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
AAE	F(10)A(11)	R
AB2	F(10)A(12)	R
AB6	F(10)A(13)	R
ABA	F(10)A(14)	R
ABE	F(10)A(15)	R
AC2	F(11)A(0)	R
AC6	F(11)A(1)	R
ACA	F(11)A(2)	R
ACE	F(11)A(3)	R
AD2	F(11)A(4)	R
AD6	F(11)A(5)	R
ADA	F(11)A(6)	R
ADE	F(11)A(7)	R
AE2	F(11)A(8)	R
AE6	F(11)A(9)	R
AEA	F(11)A(10)	R
AEE	F(11)A(11)	R
AF2	F(11)A(12)	R
AF6	F(11)A(13)	R
AFA	F(11)A(14)	R
AFE	F(11)A(15)	R
B02	F(12)A(0)	R
B06	F(12)A(1)	R
B0A	F(12)A(2)	R
B0E	F(12)A(3)	R
B12	F(12)A(4)	R
B16	F(12)A(5)	R
B1A	F(12)A(6)	R
B1E	F(12)A(7)	R
B22	F(12)A(8)	R
B26	F(12)A(9)	R
B2A	F(12)A(10)	R
B2E	F(12)A(11)	R
B32	F(12)A(12)	R
B36	F(12)A(13)	R

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
B3A	F(12)A(14)	R
B3E	F(12)A(15)	R
B42	F(13)A(0)	R
B46	F(13)A(1)	R
B4A	F(13)A(2)	R
B4E	F(13)A(3)	R
B52	F(13)A(4)	R
B56	F(13)A(5)	R
B5A	F(13)A(6)	R
B5E	F(13)A(7)	R
B62	F(13)A(8)	R
B66	F(13)A(9)	R
B6A	F(13)A(10)	R
B6E	F(13)A(11)	R
B72	F(13)A(12)	R
B76	F(13)A(13)	R
B7A	F(13)A(14)	R
B7E	F(13)A(15)	R
B82	F(14)A(0)	R
B86	F(14)A(1)	R
B8A	F(14)A(2)	R
B8E	F(14)A(3)	R
B92	F(14)A(4)	R
B96	F(14)A(5)	R
B9A	F(14)A(6)	R
39E	F(14)A(7)	R
3A2	F(14)A(8)	R
3A6	F(14)A(9)	R
3AA	F(14)A(10)	R
3AE	F(14)A(11)	R
BB2	F(14)A(12)	R
BB6	F(14)A(13)	R
BBA	F(14)A(14)	R
BBE	F(14)A(15)	R
BC2	F(15)A(0)	R

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A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
BC6	F(15)A(1)	R
BCA	F(15)A(2)	R
BCE	F(15)A(3)	R
BD2	F(15)A(4)	R
BD6	F(15)A(5)	R
BDA	F(15)A(6)	R
BDE	F(15)A(7)	R
BE2	F(15)A(8)	R
BE6	F(15)A(9)	R
BEA	F(15)A(10)	R
BEE	F(15)A(11)	R
BF2	F(15)A(12)	R
BF6	F(15)A(13)	R
BFA	F(15)A(14)	R
BFE	F(15)A(15)	R
C02	F(16)A(0)	W
C06	F(16)A(1)	W
C0A	F(16)(2)	W
C0E	F(16)A(3)	W
C12	F(16)A(4)	W
C16	F(16)A(5)	W
C1A	F(16)A(6)	W
C1E	F(16)A(7)	W
C22	F(16)A(8)	W
C26	F(16)A(9)	W
C2A	F(16)A(10)	W
C2E	F(16)A(11)	W
C32	F(16)A(12)	W
C36	F(16)A(13)	W
C3A	F(16)A(14)	W
C3E	F(16)A(15)	W
C42	F(17)A(0)	W
C46	F(17)A(1)	W
C4A	F(17)A(2)	W
C4E	F(17)A(3)	W

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
C52	F(17)A(4)	W
C56	F(17)A(5)	W
C5A	F(17)A(6)	W
C5E	F(17)A(7)	W
C62	F(17)A(8)	W
C66	F(17)A(9)	W
C6A	F(17)A(10)	W
C6E	F(17)A(11)	W
C72	F(17)A(12)	W
C76	F(17)A(13)	W
C7A	F(17)A(14)	W
C7E	F(17)A(15)	W
C82	F(18)A(0)	W
C86	F(18)A(1)	W
C8A	F(18)A(2)	W
C8E	F(18)A(3)	W
C92	F(18)A(4)	W
C96	F(18)A(5)	W
C9A	F(18)A(6)	W
C9E	F(18)A(7)	W
CA2	F(18)A(8)	W
CA6	F(18)A(9)	W
CAA	F(18)A(10)	W
CAE	F(18)A(11)	W
CB2	F(18)A(12)	W
CB6	F(18)A(13)	W
CBA	F(18)A(14)	W
CBE	F(18)A(15)	W
CC2	F(19)A(0)	W
CC6	F(19)A(1)	W
CCA	F(19)A(2)	W
CCE	F(19)A(3)	W
CD2	F(19)A(4)	W
CD6	F(19)A(5)	W
CDA	F(19)A(6)	W

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
CDE	F(19)A(7)	W
CE2	F(19)A(8)	W
CE6	F(19)A(9)	W
CEA	F(19)A(10)	W
CEE	F(19)A(11)	W
CF2	F(19)A(12)	W
CF6	F(19)A(13)	W
CFA	F(19)A(14)	W
CFE	F(19)A(15)	W
D02	F(20)A(0)	W
D06	F(20)A(1)	W
D0A	F(20)A(2)	W
D0E	F(20)A(3)	W
D12	F(20)A(4)	W
D16	F(20)A(5)	W
D1A	F(20)A(6)	W
D1E	F(20)A(7)	W
D22	F(20)A(8)	W
D26	F(20)A(9)	W
D2A	F(20)A(10)	W
D2E	F(20)A(11)	W
D32	F(20)A(12)	W
D36	F(20)A(13)	W
D3A	F(20)A(14)	W
D3E	F(20)A(15)	W
D42	F(21)A(0)	W
D46	F(21)A(1)	W
D4A	F(21)A(2)	W
D4E	F(21)A(3)	W
D52	F(21)A(4)	W
D56	F(21)A(5)	W
D5A	F(21)A(6)	W
D5E	F(21)A(7)	W
D62	F(21)A(8)	W
D66	F(21)A(9)	W

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
D6A	F(21)A(10)	W
D6E	F(21)A(11)	W
D72	F(21)A(12)	W
D76	F(21)A(13)	W
D7A	F(21)A(14)	W
D7E	F(21)A(15)	W
D82	F(22)A(0)	W
D86	F(22)A(1)	W
D8A	F(22)A(2)	W
D8E	F(22)A(3)	W
D92	F(22)A(4)	W
D96	F(22)A(5)	W
D9A	F(22)A(6)	W
D9E	F(22)A(7)	W
DA2	F(22)A(8)	W
DA6	F(22)A(9)	W
DAA	F(22)A(10)	W
DAE	F(22)A(11)	W
DB2	F(22)A(12)	W
DB6	F(22)A(13)	W
DBA	F(22)A(14)	W
DBE	F(22)A(15)	W
DC2	F(23)A(0)	W
DC6	F(23)A(1)	W
DCA	F(23)A(2)	W
DCE	F(23)A(3)	W
DD2	F(23)A(4)	W
DD6	F(23)A(5)	W
DDA	F(23)A(6)	W
DDE	F(23)A(7)	W
DE2	F(23)A(8)	W
DE6	F(23)A(9)	W
DEA	F(23)A(10)	W
DEE	F(23)A(11)	W
DF2	F(23)A(12)	W

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
DF6	F(23)A(13)	W
DFA	F(23)A(14)	W
DFE	F(23)A(15)	W
E02	F(24)A(0)	R
E06	F(24)A(1)	R
E0A	F(24)A(2)	R
E0E	F(24)A(3)	R
E12	F(24)A(4)	R
E16	F(24)A(5)	R
E1A	F(24)A(6)	R
E1E	F(24)A(7)	R
E22	F(24)A(8)	R
E26	F(24)A(9)	R
E2A	F(24)A(10)	R
E2E	F(24)A(11)	R
E32	F(24)A(12)	R
E36	F(24)A(13)	R
E3A	F(24)A(14)	R
E3E	F(24)A(15)	R
E42	F(25)A(0)	R
E46	F(25)A(1)	R
E4A	F(25)A(2)	R
E4E	F(25)A(3)	R
E52	F(25)A(4)	R
E56	F(25)A(5)	R
E5A	F(25)A(6)	R
E5E	F(25)A(7)	R
E62	F(25)A(8)	R
E66	F(25)A(9)	R
E6A	F(25)A(10)	R
E6E	F(25)A(11)	R
E72	F(25)A(12)	R
E76	F(25)A(13)	R
E7A	F(25)A(14)	R
E7E	F(25)A(15)	R

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
E82	F(26)A(0)	R
E86	F(26)A(1)	R
E8A	F(26)A(2)	R
E8E	F(26)A(3)	R
E92	F(26)A(4)	R
E96	F(26)A(5)	R
E9A	F(26)A(6)	R
E9E	F(26)A(7)	R
EA2	F(26)A(8)	R
EA6	F(26)A(9)	R
EAA	F(26)A(10)	R
EAE	F(26)A(11)	R
EB2	F(26)A(12)	R
EB6	F(26)A(13)	R
EBA	F(26)A(14)	R
EBE	F(26)A(15)	R
EC2	F(27)A(0)	R
EC6	F(27)A(1)	R
ECA	F(27)A(2)	R
ECE	F(27)A(3)	R
ED2	F(27)A(4)	R
ED6	F(27)A(5)	R
EDA	F(27)A(6)	R
EDE	F(27)A(7)	R
EE2	F(27)A(8)	R
EE6	F(27)A(9)	R
EEA	F(27)A(10)	R
EEE	F(27)A(11)	R
EF2	F(27)A(12)	R
EF6	F(27)A(13)	R
EFA	F(27)A(14)	R
EFE	F(27)A(15)	R
F02	F(28)A(0)	R
F06	F(28)A(1)	R
F0A	F(28)A(2)	R

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
F0E	F(28)A(3)	R
F12	F(28)A(4)	R
F16	F(28)A(5)	R
F1A	F(28)A(6)	R
F1E	F(28)A(7)	R
F22	F(28)A(8)	R
F26	F(28)A(9)	R
F2A	F(28)A(10)	R
F2E	F(28)A(11)	R
F32	F(28)A(12)	R
F36	F(28)A(13)	R
F3A	F(28)A(14)	R
F3E	F(28)A(15)	R
F42	F(29)A(0)	R
F46	F(29)A(1)	R
F4A	F(29)A(2)	R
F4E	F(29)A(3)	R
F52	F(29)A(4)	R
F56	F(29)A(5)	R
F5A	F(29)A(6)	R
F5E	F(29)A(7)	R
F62	F(29)A(8)	R
F66	F(29)A(9)	R
F6A	F(29)A(10)	R
F6E	F(29)A(11)	R
F72	F(29)A(12)	R
F76	F(29)A(13)	R
F7A	F(29)A(14)	R
F7E	F(29)A(15)	R
F82	F(30)A(0)	R
F86	F(30)A(1)	R
F8A	F(30)A(2)	R
F8E	F(30)A(3)	R
F92	F(30)A(4)	R
F96	F(30)A(5)	R

A24 Offset$_{16}$	CAMAC F/A	REGISTER ACCESS
F9A	F(30)A(6)	R
F9E	F(30)A(7)	R
FA2	F(30)A(8)	R
FA6	F(30)A(9)	R
FAA	F(30)A(10)	R
FAE	F(30)A(11)	R
FB2	F(30)A(12)	R
FB6	F(30)A(13)	R
FBA	F(30)A(14)	R
FBE	F(30)A(15)	R
FC2	F(31)A(0)	R
FC6	F(31)A(1)	R
FCA	F(31)A(2)	R
FCE	F(31)A(3)	R
FD2	F(31)A(4)	R
FD6	F(31)A(5)	R
FDA	F(31)A(6)	R
FDE	F(31)A(7)	R
FE2	F(31)A(8)	R
FE6	F(31)A(9)	R
FEA	F(31)A(10)	R
FEE	F(31)A(11)	R
FF2	F(31)A(12)	R
FF6	F(31)A(13)	R
FFA	F(31)A(14)	R
FFE	F(31)A(15)	R

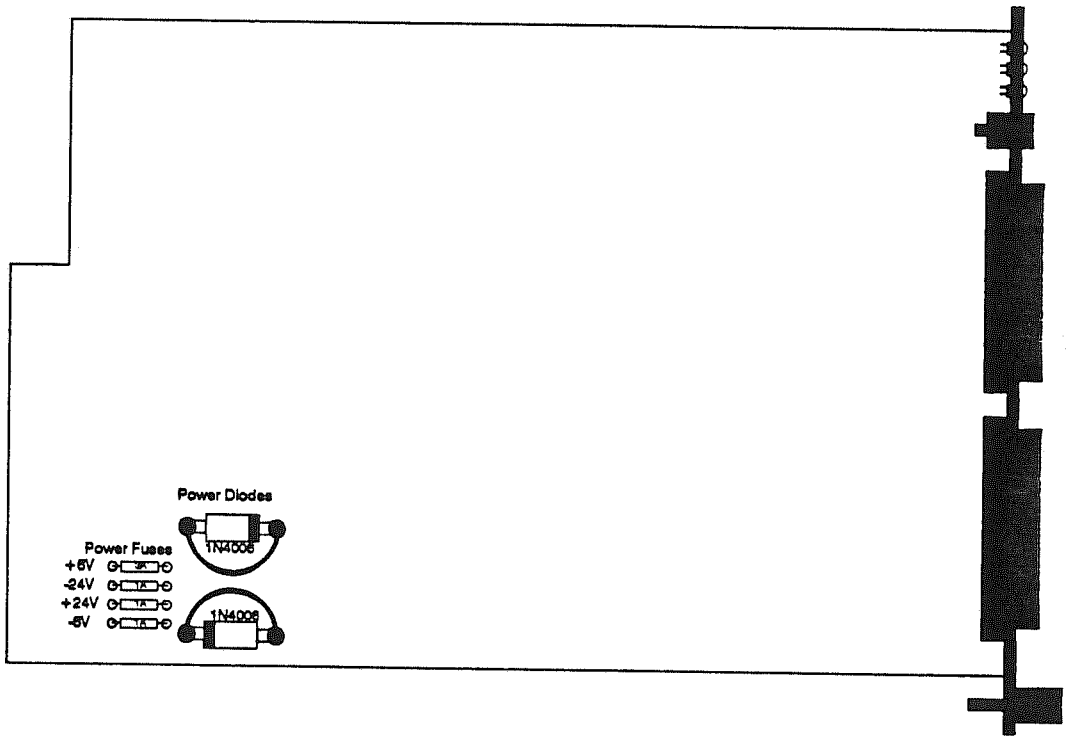

FIGURE 2 - V500 STRAP LOCATIONS