Model V525

VXIbus Development Module

**INSTRUCTION MANUAL**

February, 1999

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# VXIbus Development Module

## An ideal platform to create a custom module

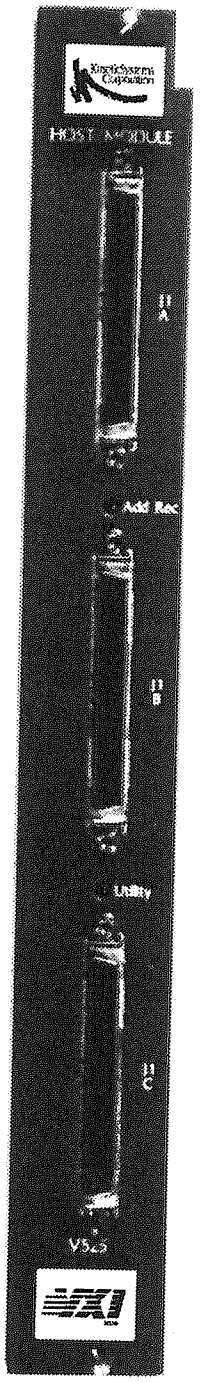
# V525

### Features

- **Single-width VXI module**
- **VXI register-based interface**
- **Strap-selectable power and ground arrays**
- **Provisions for up to 3 plug-in development cards**
- **Front panel hardware, connectors, and shields are included**

### Typical Applications

- **Product development and prototyping**
- **Custom products**



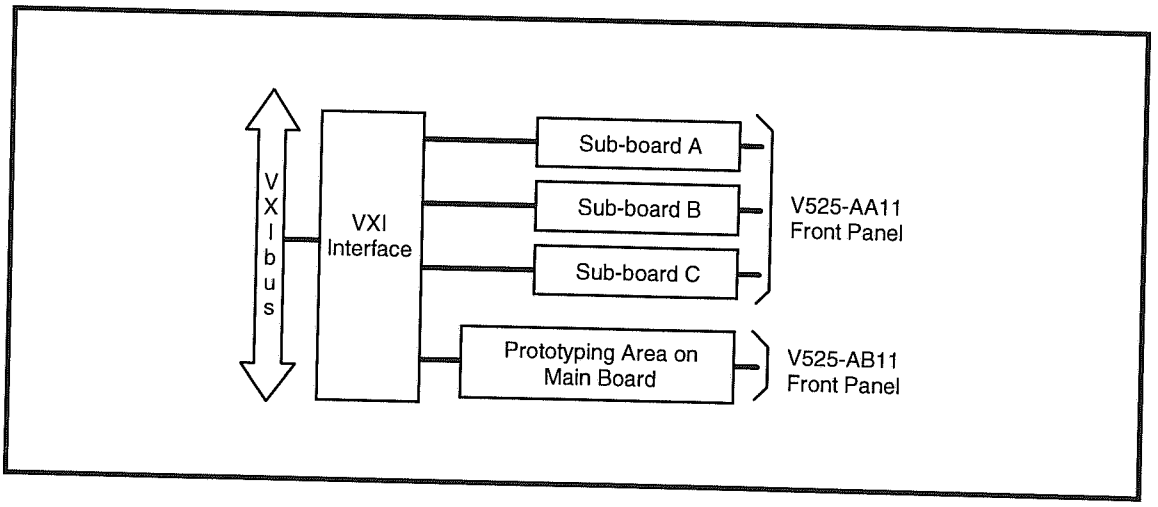
### General Description **(Product specifications and descriptions subject to change without notice.)**

The V525 is a single-width, C-size, VXIbus module that provides a prototyping and development platform consisting of a standard, VXI, register-based interface and an array of holes for circuit breadboarding. Power and ground are strap-selectable to points within the array of holes that allow for IC packages with 0.3" and 0.6" pin spacing as well as spacing for PGA sockets up to 17 pins per side. In addition, six 50-position, interboard connectors are provided on the host module which carry VXIbus address, data, control, power, and ground signals. These connectors allow the user to develop circuitry on up to three plug-in submodule cards for reconfigurable or higher density applications.

The register-based VXI interface on the V525 provides the configuration registers required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. Access to the configuration registers is available through the VMEbus Short Address (A16) Space. The V525 supports both static and dynamic configuration. Additionally, circuitry is provided to interface to user-supplied operational registers positioned in VMEbus Standard Address (A24) Space.

The V525-AA11 option includes a front-panel that accepts three submodules with 68P High Density connectors. Sufficient interface and physical information is available to allow you to develop custom submodules. The V525-AB11 option includes a front panel and two 68P High Density board mounted connectors on the host module. LED indicators for address recognition and utility purposes as well as left and right-side ground shields are provided on both options

### V525 Interface Paths

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| Item | Specification |
|---|---|
| Interface Power Requirements | |
| +5 V | 1 A |
| Power Available to Breadboard/Submodules | *Note: Total available mainframe power must also be checked .* |
| +5 V | 6 A max. |
| -5.2 V | 5 A max. |
| -2 V | 2 A max. |
| +12 V | 1 A max. |
| -12 V | 1 A max. |
| +24 V | 1 A max |
| -24 V | 1 A max |
| +15 V | TBD mA max. |
| -15 V | TBD mA max. |
| Environmental and Mechanical | |
| Temperature range | |
| Operational | 0°C to 50°C |
| Storage | -25°C to +75°C |
| Relative Humidity | 0 to 85%, non-condensing to 40°C |
| Cooling Requirements | 10 CFM |
| Dimensions | 340 mm x 233.35 mm x 30.48 mm (V-size VXIbus) |
| Front-panel potential | Chassis Ground |

## Ordering Information

Model V525-AA11 VXIbus Development Module with submodule connector front-panel option
Model V525-AB11 VXIbus Development Module with host module connector front-panel option

Note: Each V525-AA11 includes connectors for 3 custom submodules. The submodules are not included. However, sufficient interface and physical information is available to allow you to develop custom submodules.

## UNPACKING AND INSTALLATION

The Model V525 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the operating environment.

### Logical Address Switches

The V525 represents one of the 255 devices permitted in a VXI*bus* system. (Logical Address 0 is reserved for the Slot 0 device.) The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V525 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. (Refer to Figure 1.)

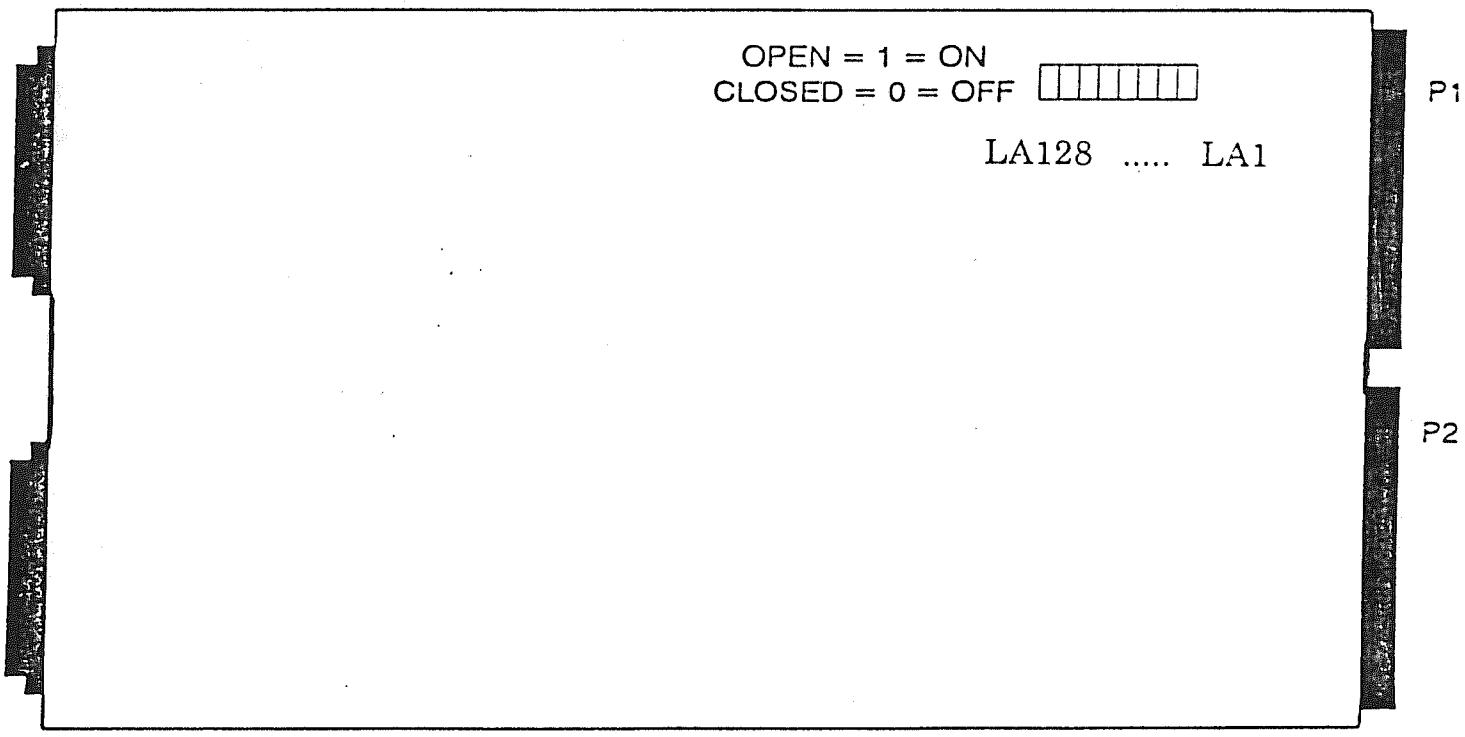



FIGURE 1 - V525 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the A16 base address is shown below:

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | LA 128 | LA 64 | LA 32 | LA 16 | LA 8 | LA 4 | LA 2 | LA 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 15 and 14 are set to one (VXI defined).

Bits 13 through 6 are user-selectable via the address switches LA128-LA1.

Bits 5 through zero are set to "0" to indicate a block of 64 words.

### Module Insertion

The V525 is a C-sized, single-width VXI*bus* module. It requires 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-sized VXI*bus* mainframe.

| | |
|---|---|
| **CAUTION:** | **TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE** |

| | |
|---|---|
| **WARNING:** | **REMEMBER TO REMOVE THE INTERRUPT ACKNOWLEDGE DAISYCHAIN JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE** |

To insure proper interrupt acknowledge cycles through the V525 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot.

## FRONT PANEL INFORMATION

### LEDs

| | |
|---|---|
| Add Rec | This LED turns on when any of the V525 registers are being accessed. |
| Utility | This LED is undedicated and may be driven by a user-defined TTL low-level signal. Access to this LED is available at each of the 50-position submodule J2 connectors at pin 26 (refer to Table 1). |

## Front Panel Connections

The V525-AA11 front panel has cutouts that accept three submodule mounted 68-position SCSI-II type receptacle connectors labeled J1A, J1B, and J1C. (Submodules are not included with the V525-AA11 option.) The V525-AB11 is provided with two 68-position SCSI-II type plug connectors labeled P3 and P4. Access to these connector pins is provided in the form of an array of holes to which wires from the breadboard area can be routed. The contact layout for these connectors is shown in Figure 2.

## Configuration of Module Straps

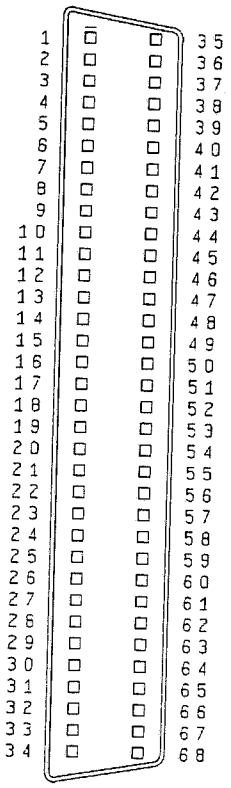
There are a number of user configurable straps on the V525. Refer to Figure 3, for the location of these straps.

Straps V1 through V16 are user configured in order to provide the desired power supply voltage or ground to the 16 horizontal rows of holes that are marked with a white box within the breadboard area. Solder 1 strap per row into the location marked with the desired power supply voltage or ground. Sixteen 0.1 inch straps are provided with the V525 for this purpose.

The V525 VXI*bus* interface circuitry supports 16-bit and 24-bit addressing (A16 and A24) as well as 16-bit (D16) data transfers. In addition, there are provisions in the form of address/data line access holes and address/data configuration straps that give the user the option of developing circuitry to perform 32-bit data transfers and 32-bit address decoding. For normal A16/A24 operations the configuration straps should be left in the factory default positions of Standard I/O (S), A24 address compare match (M1) and EEPROM disabled (D). For user developed A16/A32 circuitry the straps should be moved to the Extended I/O (E) and user address compare match (M2) positions. Also, the EEPROM strap must be moved to the enabled (E) position and the appropriate data should be written to the ID and Device Type configuration registers to ensure proper system configuration. The EEPROM strap should then be returned to the disabled (D) position. Refer to the Register Layout section for more information on the ID and Device Type registers.

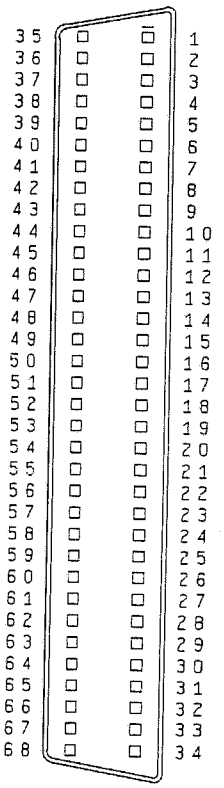
The Hostmodule DTACK/Submodule DTACK strap gives users the option of developing their own DTACK timing circuitry or using the DTACK circuitry provided by the V525's interface. When implementing a user-developed DTACK source the strap should be placed in the Submodule DTACK position. When using the V525 interface's DTACK source the strap should be in the Hostmodule DTACK position. See Figure 4, for the V525 interface DTACK timing diagrams.

68-Contact High Density
(SCSI II Type) Receptacle




Front View
V525-AA11 Option
Reversed Mounting Position
For Submodule or Daughter Card

68-Contact High Density
(SCSI II Type) Plug




Front View
V525-AB11 Option
Standard Mounting Position

**Figure 2 - V525 Front Panel Connector Contact Orientation**

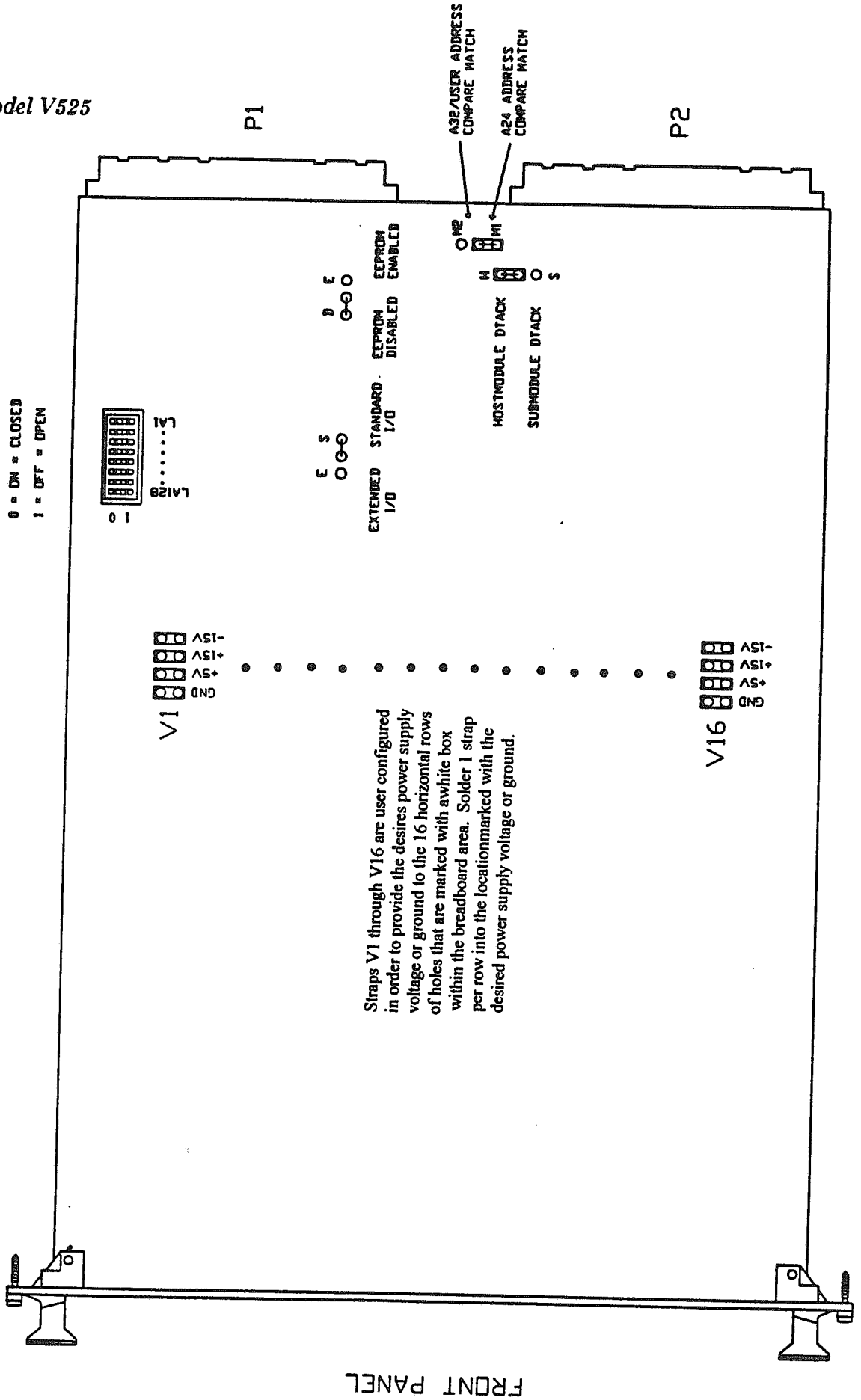
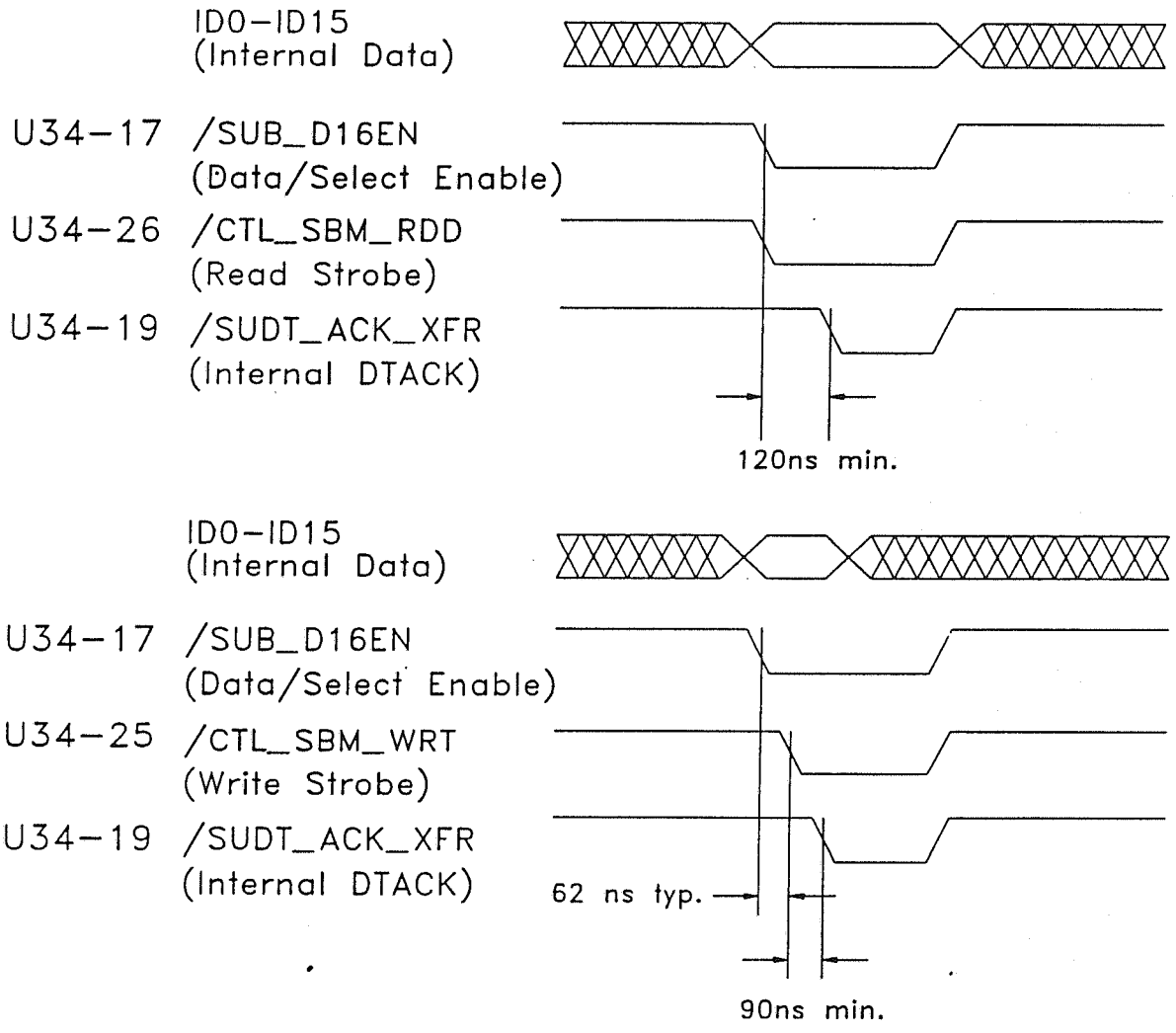



**Figure 3 - V525 Strap Locations**

V525 Submodule Interface Read/Write Strobe to DTACK Timing
for Factory Provided DTACK Circuit
Device Number P0461 Location U34




Note: The maximum propagation time for the data path between the VXIbus backplane and the internal data bus is 8ns. The minimum propagation time from internal DTACK to DTACK at the VXIbus backplane is 6ns.

**Figure 4 - V525 Submodule Interface**

## Circuit Breadboard Area Power and Ground

The V525 VXI*bus* Development Module provides an array of holes for circuit breadboarding. Power and ground are strap-selectable to points within the array of holes that allow for IC packages with 0.3" and 0.6" pin spacing as well as spacing for PGA sockets up to 17 pins per side. In addition, six 50-position, interboard connectors are provided which carry power and ground to optional plug-in submodule cards. See the Configuration of Module Straps section for information on configuring power and ground to the breadboard area.

## Circuit Breadboard Area Signal Wiring

In addition to the array of holes for circuit breadboarding, solder-type wiring holes are provided on the V525 for access to buffered VXI*bus* address, data, and other key signals. Figure 5 may be used in conjunction with the V525 circuit schematics to cross-reference the wiring access-hole silkscreen labels to the signals present at these holes.

## Submodule Applications

Six 50-position interboard connectors are provided on the V525 hostmodule that allow the user to develop circuitry on up to three plug-in submodule cards for reconfigurable or high density applications. Access to the data strobes, buffered system clock, DTACK, and other signals., is available at the six interboard connector locations J2 A, B, C and J3 A, B, C. (Refer to the circuit schematics or the submodule interboard connector pinout tables for additional signal pinout information). VXIbus address lines A11 and A12 are decoded to provide submodule select lines for accessing registers implemented on the optional submodules, as shown in the table below:

| IA12 | IA11 | |
|---|---|---|
| 0 | 0 | Select submodule "A" (Signal/SEL_SBF:1 at connector J3A, Pin 9, is LOW) |
| 0 | 1 | Select submodule "B" (Signal/SEL_SBF:2 at connector J3B, Pin 9, is LOW) |
| 1 | 0 | Select submodule "C" (Signal/SEL_SBF:3 at connector J3C, Pin 9, is LOW) |
| 1 | 1 | Select all submodules "A,B,C" (Signal/SEL_SBF:4 at Pin 10 of connectors J3A, J3B, and J3C is LOW) |

## Table 1 - V525-AA11, AB11 Interboard Connector Pinouts

Connector J2: There are three J2 connectors (A. B, C) with identical pinouts.

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | No Connection | 2 | Ground |
| 3 | No Connection | 4 | Ground |
| 5 | No Connection | 6 | Ground |
| 7 | No Connection | 8 | Ground |
| 9 | DataIO_B01 | 10 | Ground |
| 11 | DataIO_B02 | 12 | +24v |
| 13 | DataIO_B03 | 14 | Ground |
| 15 | DataI0_B04 | 16 | Ground |
| 17 | DataIO_B05 | 18 | +12v |
| 19 | DataIO_B06 | 20 | Ground |
| 21 | DataIO_B07 | 22 | +5v |
| 23 | DataIO_B08 | 24 | Ground |
| 25 | DataIO_B09 | 26 | Util_Led |
| 27 | DataIO_B10 | 28 | Ground |
| 29 | DataIO_B11 | 30 | -5v |
| 31 | DataIO_B12 | 32 | Ground |
| 33 | DataIO_B13 | 34 | -12v |
| 35 | DataIO_B14 | 36 | Ground |
| 37 | DataIO_B15 | 38 | Ground |
| 39 | DataIO_B16 | 40 | -24v |
| 41 | BUS_SBM_L01 | 42 | Ground |
| 43 | BUS_SBM_L02 | 44 | Ground |
| 45 | BUS_SBM_L03 | 46 | Ground |
| 47 | BUS_SBM_L04 | 48 | Ground |
| 49 | CLK_VXI_16M | 50 | Ground |

**Table 2 - V525-AA11, AB11 Interboard Connector Pinouts**

Connector J3: There are three J3 connectors (A, B, C) that have identical pinouts with the exception of J3 pin 9 which is used to select a given submodule.

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | No Connection | 2 | Ground |
| 3 | No Connection | 4 | Ground |
| 5 | No Connection | 6 | Ground |
| 7 | No Connection | 8 | Ground |
| 9 | SEL_SBF:n | 10 | SEL_SBF:4 |
| 11 | ADF_VXI_LWD | 12 | +24v |
| 13 | ADF_VXI_DS0 | 14 | Ground |
| 15 | ADF_VXI_DS1 | 16 | Ground |
| 17 | ADR_VXI_A01 | 18 | +12v |
| 19 | ADR_VXI_A02 | 20 | Ground |
| 21 | ADR_VXI_A03 | 22 | +5v |
| 23 | ADR_VXI_A04 | 24 | Ground |
| 25 | ADR_VXI_A05 | 26 | Sys_Reset |
| 27 | ADR_VXI_A06 | 28 | Ground |
| 29 | ADR_VXI_A07 | 30 | -5v |
| 31 | ADR_VXI_A08 | 32 | Ground |
| 33 | ADR_VXI_A09 | 34 | -12v |
| 35 | ADR_VXI_A10 | 36 | Ground |
| 37 | CTL-SBM_RDD | 38 | CTL_SBM_WRT |
| 39 | UDT_ACK_XRF | 40 | -24v |
| 41 | BUS_SBM_L05 | 42 | Ground |
| 43 | BUS_SBM_L06 | 44 | Ground |
| 45 | BUS_SBM_L07 | 46 | Ground |
| 47 | BUS_SBM_L08 | 48 | Ground |
| 49 | ITR_DSP_SBM | 50 | Ground |

## PROGRAMMING INFORMATION

### VMEbus/VXIbus Addressing

Of the defined VXI*bus* Configuration Registers, the V525 implements those required for extended, register-based devices.

Access to the Configuration Registers for all VXI*bus* modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

### VXIbus Configuration Registers

Configuration Registers are required by the VXI*bus* specification so that the appropriate level of system configuration can be accomplished. The Configuration Registers in the V525 are offset from the base address. **Note: the V525 only responds to these addresses if the Short Nonpriviledged Access ($29_{16}$) or Short Supervisory Access ($2D_{16}$ ) Address Modifier Codes are set for the backplane bus cycle.** Table 3 shows the applicable Configuration Registers present in the V525, their offset from the base (Logical) address, and their Read/Write capabilities.

**Table 3. Configuration Registers Short Address (A16) Space**

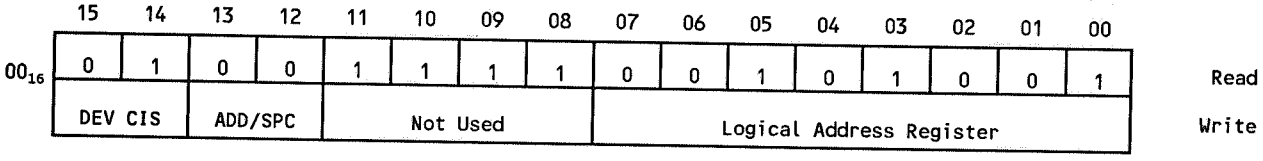
| A16 Offset | Read/Write Capability | Register Name |
|---|---|---|
| $00_{16}$ | Read/Write | ID/Logical Address Register |
| $02_{16}$ | Read Only | Device Type Register |
| $04_{16}$ | Read/Write | Status/Control Register |
| $06_{16}$ | Read/Write | Offset Register |
| $08_{16}$ | Read Only | Attribute Register |
| $0A_{16}$ | Read Only | Serial Number High Register |
| $0C_{16}$ | Read Only | Serial Number Low Register |
| $0E_{16}$ | Read Only | Version Number Register |
| $10_{16}$ - $19_{16}$ | Read Only | Reserved |
| $1A_{16}$ | Read Only | Interrupt Status Register |
| $1C_{16}$ | Read/Write | Interrupt Control Register |
| $1E_{16}$ | Read Only | Subclass Register |
| $20_{16}$ | Read Only | Suffix Register High |
| $22_{16}$ | Read Only | Suffix Register Low |
| $24_{16}$ - $3F_{16}$ | Read/Write | User Defined |

*Model V525*

## REGISTER LAYOUT

### ID/Logical Address Register

The format and bit assignments for the ID/Logical Address register are as follows:



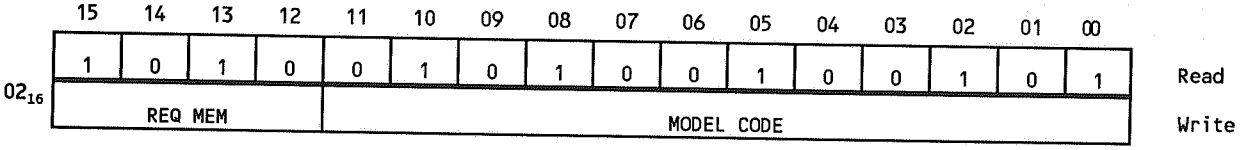

On READ transactions:

| Bit(s) | Mnemonic | Meaning |
|---|---|---|
| 15, 14 | Device Class | This is an Extended Register-Based device. |
| 13, 12 | Address Space Needs | This module requires the use of A16/A24 address space. |
| 11 - 00 | Manufacturer's ID | 3881 ($F29_{16}$) for KineticSystems. |

For WRITE transactions, bits fifteen through eight are not used. A write to these bits has no effect on the V525. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

### Device Type Register

The format and bit assignments for the Device Type register are as follows:

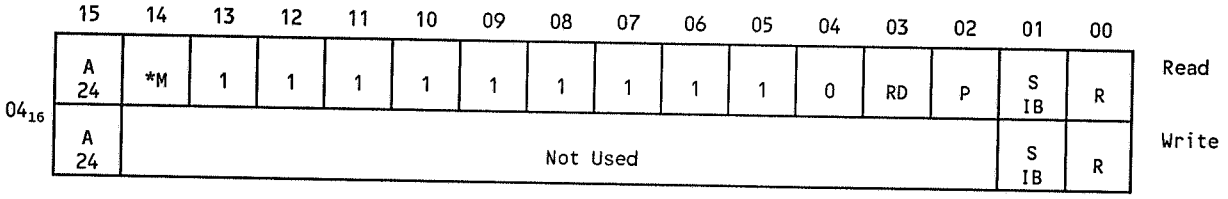



On READ/WRITE transactions:

| Bit(s) | Mnemonic | Meaning |
|---|---|---|
| 15 - 12 | Required Memory | The V525 requires 8K bytes of additional memory space. |
| 11 - 0 | Model Code | Identifies this device as Model V525 ($525_{16}$). |

## Status/Control Register

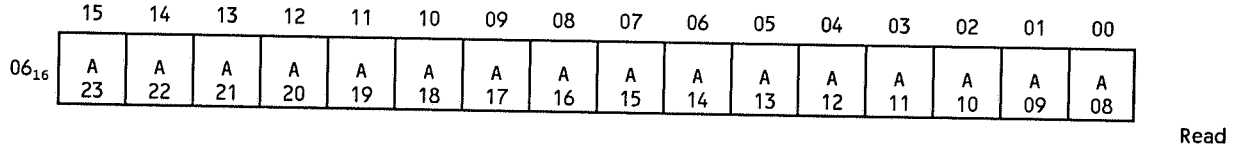
The format and bit assignments for the Status/Control register are as follows:




| Bit(s) | Mnemonic | Meaning |
|---|---|---|
| 15 | A24 | This bit is written with a "1" to enable A24 addressing and reset (to "0") to disable A24 addressing. **This bit <u>must</u> be set to "1" to allow access to the module's Operational (A24) Registers.** Reading this bit indicates its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET* |
| 14 | Modid* | This read only bit is set to a "1" if the module is <u>not</u> selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line. |
| 13 - 04 | Not used. | When read will return all "1"s. These bits are ignored when written. |
| 03 | Ready | A "1" indicates the successful completion of register initialization. This bit is read only. |
| 02 | Pass | When read will return a "1". Self-test is not implemented on the V525. |
| 01 | Sysfail Inhibit | Writing a "1" to this bit disables the device from driving the SYSFAIL* line. Reads of this bit indicate its current state. |
| 00 | Reset | Writing a "1" to this bit forces the device into the Soft Reset condition. While in the Soft Reset state, the module will only allow accesses to Configuration Registers. This bit must be cleared along with the Passed and Ready bits set before any access to the Operational (A24) Registers is allowed. |

### Offset Register

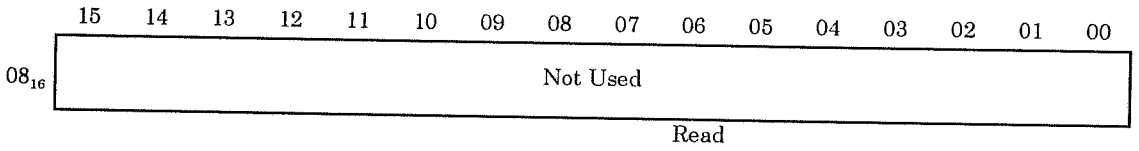
The format and bit assignments for the Offset Type register are as follows:




After SYSRESET* all bits are set to "0". Otherwise, a read or write defines the base address of the device's A24 operational registers.

### Attribute Register

The format and bit assignments for the Attribute register are as follows:




| Bit(s) | Mnemonic | Meaning |
|---|---|---|
| 15 - 00 | Not used | A write to these bits has no effect. A read of these bits will return all "" 1"s". |

As shipped, the V525 does not report the use or capability of generating VXI interrupts. In order for designs that use interrupts to function properly the Attribute Register will need to be reprogrammed. Please refer to the VXI standard manual for more information on the use and implementation of VXI interrupts. The bit assignments and definition are shown below:

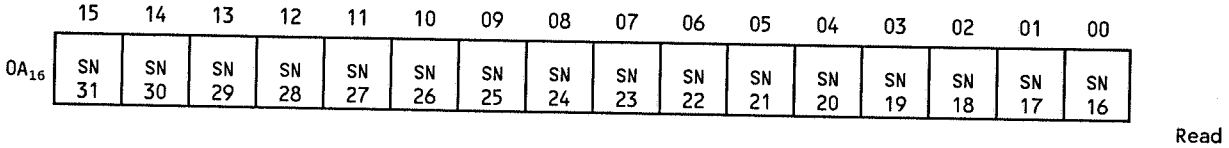
Bit 0:IS — Indicates the device has Interrupt Status Reporting capability. (A zero indicates the option is implemented. A one indicates option is not implemented.)

Bit 1:IH — Indicates the device has Interrupt Handler Control capability. (A zero indicates the option is implemented. A one indicates option is not implemented.)

Bit 2:IR — Indicates the device has Interrupt Control capability. (A zero indicates the option is implemented. A one indicates option is not implemented.)

### Serial Number High Register

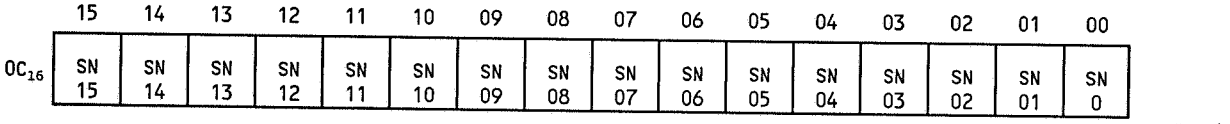
The format and bit assignments for the Serial Number High register are as follows:




This read only register contains the upper code of the module's serial number.

### Serial Number Low Register

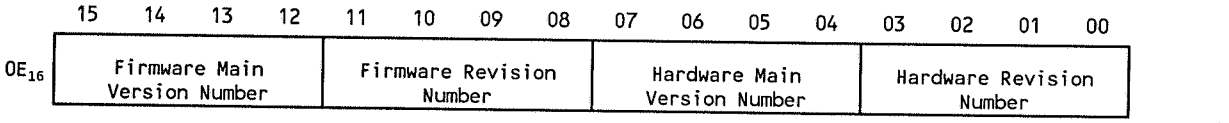
The format and bit assignments for the Serial Number Low register are as follows:




This read only register contains the lower code of the module's serial number.

### Version Number Register

The format and bit assignments for the Version Number register are as follows:



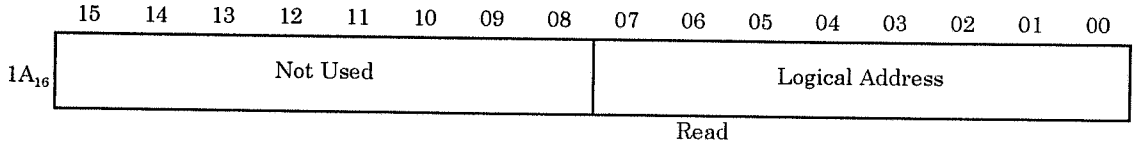

The following patterns are given as an example. The values read will reflect the current revision of the module.

| Bit(s) | Mnemonic | Meaning |
|---|---|---|
| 15 - 12 | Firmware Main Version Number | $1_{16}$ |
| 11 - 08 | Firmware Revision Number | $0_{16}$ |
| 07 - 04 | Hardware Main Version Number | $1_{16}$ |
| 03 - 00 | Hardware Revision Number | $0_{16}$ |

### $10_{16}$ - $19_{16}$ Reserved

### Interrupt Status Register

The format and bit assignments for the Interrupt Status register are as follows:

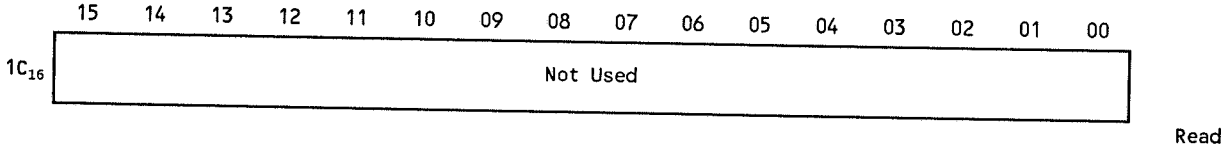


This following bit patterns will be returned during a read of this register.

| Bit(s) | Mnemonic | Meaning |
|---|---|---|
| 15 - 08 | Not Used | These bits are read as ""1"s". |
| 07 - 00 | Logical Address | Logical address of the device. |

### Interrupt Control Register

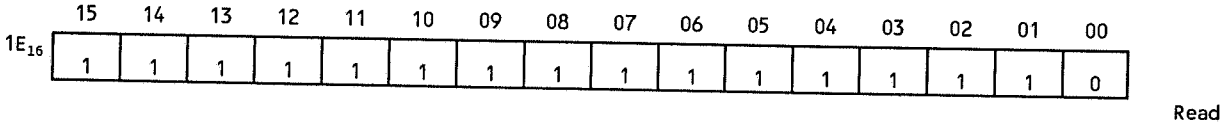
The format and bit assignments for the Interrupt Control register are as follows:




Note: The V525 does not support any interrupt capabilities. For compatibility with other KineticSystems modules, this register is retained. This register should be written with all "1"s.

### Subclass Register

The format and bit assignments for the Subclass register are as follows:

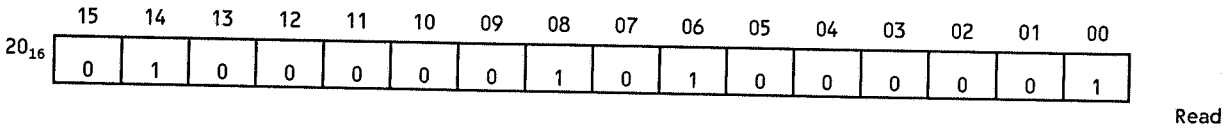



| Bit(s) | Meaning |
|---|---|
| 15 | VXIbus extended device |
| 14 - 0 | $7FFE_{16}$ - Extended Register Based Device |

The following two registers contain the ASCII equivalent of the module suffix. This suffix contains the information needed to determine the option of the module. The examples given below are for a V525-AA11 (Development Module Option). Refer to the Ordering Information to determine the option and its corresponding suffix.

### Suffix Register High

The format and bit assignments for the Suffix Register High are as follows:




This read only register contains the upper code of the module's suffix (ZA = $4141_{16}$).

### Suffix Register Low

The format and bit assignments for the Suffix Register Low are as follows:

| | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $22_{16}$ | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

Read

This read only register contains the upper code of the module's suffix (11 = $3131_{16}$).

### $24_{16}$-$3F_{16}$ User Defined

These Write/Read registers are contained in non-volatile EEPROM and may be used to store user defined data. Allow 10 milliseconds for writes to these registers.

## OPTION DESCRIPTIONS

**Model V525-AA11** - VXI*bus* Development Module with front panel option to accept three submodules with 68-contact high density plug connectors.

**Model V525-AB11** - VXI*bus* Development Module with front panel option for two hostmodule boards mounted with 68-contact high density plug connectors.

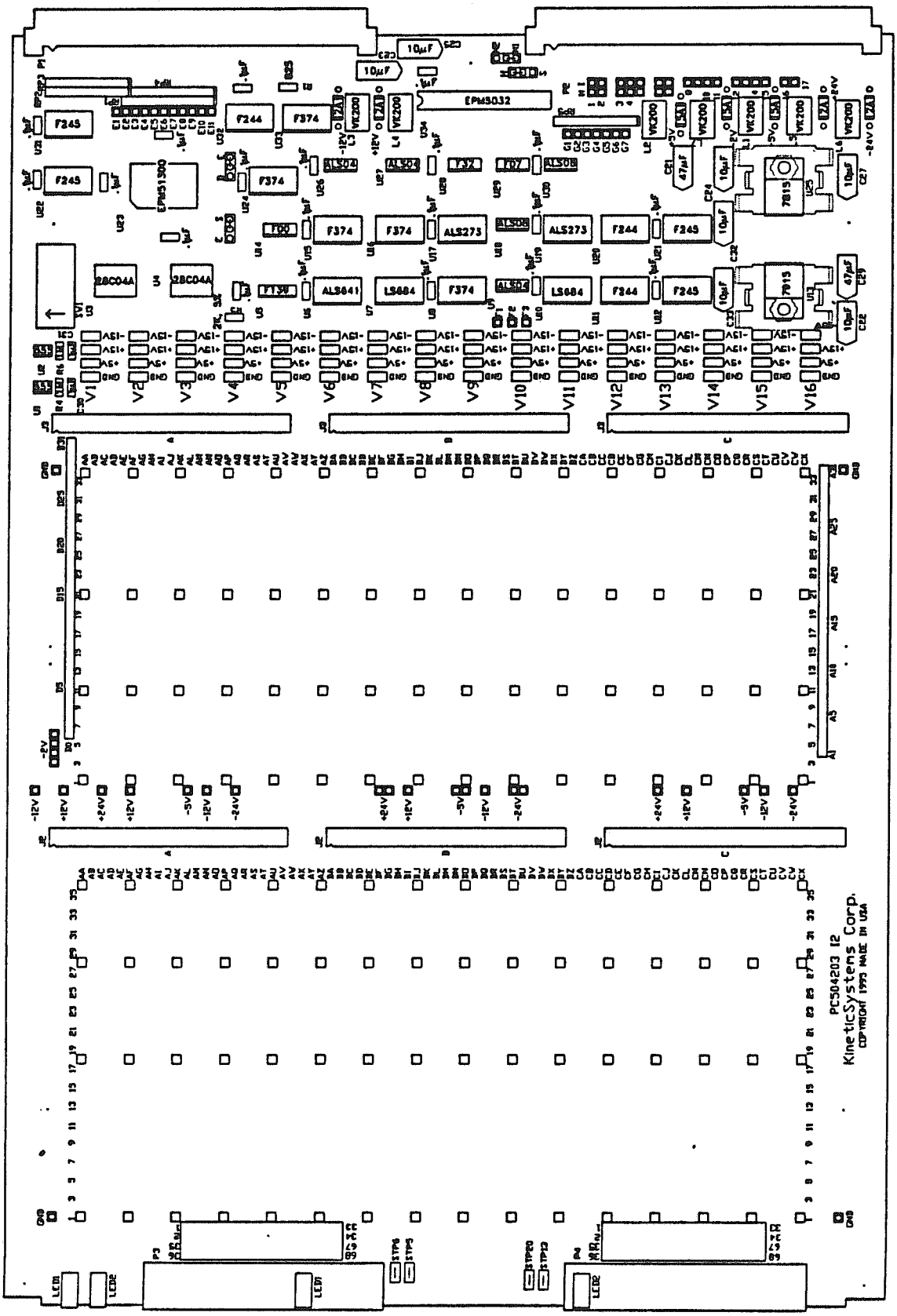



**Figure 5 - V525 Module**

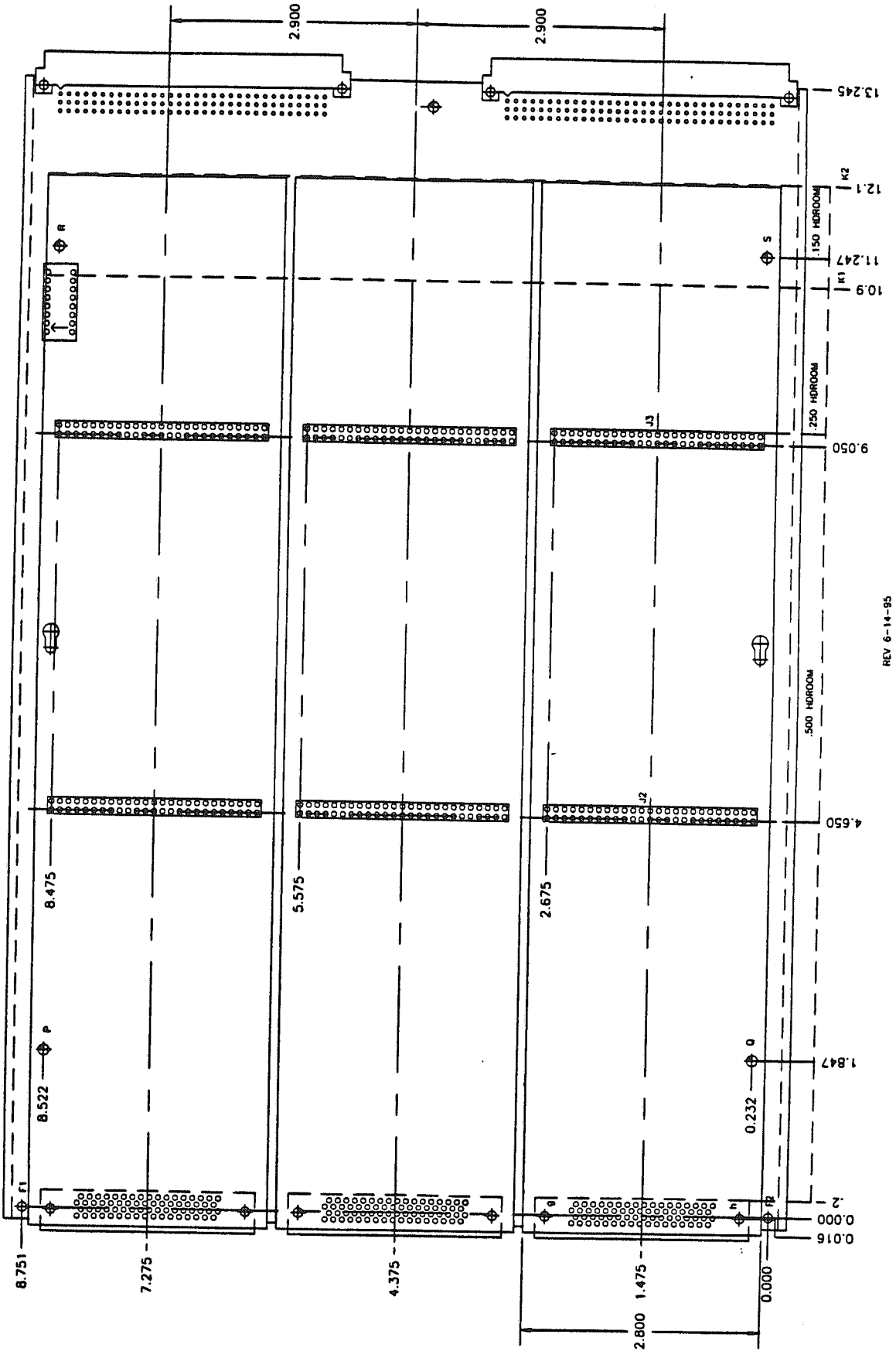



**Figure 6 - V525 Mechanical Drawing**

## Submodule and Hostmodule Connectors

**TSS-125-02-S-D** **SAMTEC, 1995 Catalog, pg 34-35** **Submodule**

| | |
|---|---|
| TSS | Top-Shrounded 0.025-in Square-Post Maile-Pin Strip |
| 125 | 25-positions on 0.100-in Centers |
| 02 | Lead Style: Tail Length = 0.165-in |
| S | Plating Option: Gold-Ctk/Tin-Tail |
| D | Double-Row Contacts, Total 50-Ctks |
| | Body Height = 0.350 + 0.015-in = 0.365-in |
| NOTE: | Insertion Depth = 0.25-in; Tail-Length is compatible with intended PWB-Thickness = 0.093 to 0.125-in. |

**SSW-125-22-S-D** **SAMTEC, 1995 Catalog, pg 40-41** **Hostmodule**

| | |
|---|---|
| SSW | Socket Strip, Solder-Tail: 0.016 x 0.031-in |
| 125 | 25-positions on 0.100-in Centers |
| 22 | 0.190-in Contact-Tail Length, LIF/LWF: 3.0/2.6-oz |
| S | Plating Option: Gold-Ctk/Tin-Tail |
| D | Double-Row Contacts, Total 50-Ctks |
| NOTE: | Body Height = 0.335-in; Tail-length is compatible with intended PWB-Thickness = 0.063-in. |

**Table 4. Additional Available Signals**

| Silkscreen Label | Schematic Label | Signal Description |
|---|---|---|
| A1 | IA1 | Internally buffered address line A01 |
| A2 | IA2 | Internally buffered address line A02 |
| A3 | IA3 | Internally buffered address line A03 |
| A4 | IA4 | Internally buffered address line A04 |
| A5 | IA5 | Internally buffered address line A05 |
| A6 | IA6 | Internally buffered address line A06 |
| A7 | IA7 | Internally buffered address line A07 |
| A8 | IA8 | Internally buffered address line A08 |
| A9 | IA9 | Internally buffered address line A09 |
| A10 | IA10 | Internally buffered address line A10 |
| A11 | IA11 | Internally buffered address line A11 |
| A12 | IA12 | Internally buffered address line A12 |
| A13 | IA13 | Internally buffered address line A13 |
| A14 | IA14 | Internally buffered address line A14 |
| A15 | IA15 | Internally buffered address line A15 |
| A16 | IA16 | Internally buffered address line A16 |
| A17 | IA17 | Internally buffered address line A17 |
| A18 | IA18 | Internally buffered address line A18 |
| A19 | IA19 | Internally buffered address line A19 |
| A20 | IA20 | Internally buffered address line A20 |
| A21 | IA21 | Internally buffered address line A21 |
| A22 | IA22 | Internally buffered address line A22 |
| A23 | IA23 | Internally buffered address line A23 |
| A24 | IA24 | Internally buffered address line A24 |
| A25 | IA25 | Internally buffered address line A25 |
| A26 | IA26 | Internally buffered address line A26 |
| A27 | IA27 | Internally buffered address line A27 |
| A28 | IA28 | Internally buffered address line A28 |
| A29 | IA29 | Internally buffered address line A29 |

| | | |
|---|---|---|
| A30 | IA30 | Internally buffered address line A30 |
| A31 | IA31 | Internally buffered address line A31 |
| D0 | ID0 | Internally buffered data line D00 |
| D1 | ID1 | Internally buffered data line D01 |
| D2 | ID2 | Internally buffered data line D02 |
| D3 | ID3 | Internally buffered data line D03 |
| D4 | ID4 | Internally buffered dat a line D04 |
| D5 | ID5 | Internally buffered data line D05 |
| D6 | ID6 | Internally buffered data line D06 |
| D7 | ID7 | Internally buffered data line D07 |
| D8 | ID8 | Internally buffered data line D08 |
| D9 | ID9 | Internally buffered data line D09 |
| D10 | ID10 | Internally buffered data line D10 |
| D11 | ID11 | Internally buffered data line D11 |
| D12 | ID12 | Internally buffered data line D12 |
| D13 | ID13 | Internally buffered data line D13 |
| D14 | ID14 | Internally buffered data line D14 |
| D15 | ID15 | Internally buffered data line D15 |
| D16 | ID16 | Internally buffered data line D16 |
| D17 | ID17 | Internally buffered data line D17 |
| D18 | ID18 | Internally buffered data line D18 |
| D19 | ID19 | Internally buffered data line D19 |
| D20 | ID20 | Internally buffered data line D20 |
| D21 | ID21 | Internally buffered data line D21 |
| D22 | ID22 | Internally buffered data line D22 |
| D23 | ID23 | Internally buffered data line D23 |
| D24 | ID24 | Internally buffered data line D24 |
| D25 | ID25 | Internally buffered data line D25 |
| D26 | ID26 | Internally buffered data line D26 |
| D27 | ID27 | Internally buffered data line D27 |
| D28 | ID28 | Internally buffered data line D28 |
| D29 | ID29 | Internally buffered data line D29 |

| | | |
|---|---|---|
| D30 | ID30 | Internally buffered data line D30 |
| D31 | ID31 | Internally buffered data line D31 |
| E1 | INTSRC7 | Internal interrupt source line 7 |
| E2 | INTSRC6 | Internal interrupt source line 6 |
| E3 | RD_INSTAT | Read interrupt status |
| E4 | INTSRC5 | Internal interrupt source line 5 |
| E5 | INTSRC4 | Internal interrupt source line 4 |
| E6 | INTSRC3 | Internal interrupt source line 3 |
| E7 | STAND_BLT | Standard block transfer |
| E8 | INTSRC2 | Internal interrupt source line 2 |
| E9 | INTSRC1 | Internal interrupt source line 1 |
| E10 | INTSRC0 | Internal interrupt source line 0 |
| E11 | EXT_BLT | Extended block transfer |
| F1 | MATCH2 | User address compare match |
| F2 | RESET | Internal reset |
| F3 | WR_OFF | Write offset |
| G1 | TTL_TRG1 | Internal TTL trigger line 1 |
| G2 | TTL_TRG2 | Internal TTL trigger line 2 |
| G3 | TTL_TRG3 | Internal TTL trigger line 3 |
| G4 | TTL_TRG4 | Internal TTL trigger line 4 |
| G5 | TTL_TRG5 | Internal TTL trigger line 5 |
| G6 | TTL_TRG6 | Internal TTL trigger line 6 |
| G7 | TTL_TRG7 | Internal TTL trigger line 7 |
| H1 | LBUSC00 | Local Bus line C00 |
| H2 | LBUSC01 | Local Bus line C01 |
| H3 | LBUSC02 | Local Bus line C02 |
| H4 | LBUSC03 | Local Bus line C03 |
| H5 | LBUSC04 | Local Bus line C04 |
| H6 | LBUSC05 | Local Bus line C05 |
| H7 | LBUSC06 | Local Bus line C06 |
| I1 | LBUSA00 | Local Bus line A00 |
| I2 | LBUSA01 | Local Bus line A01 |

| | | |
|---|---|---|
| I3 | LBUSA02 | Local Bus line A02 |
| I4 | LBUSA03 | Local Bus line A03 |
| I5 | LBUSA04 | Local Bus line A04 |
| I6 | LBUSA05 | Local Bus line A05 |
| I7 | LBUSA06 | Local Bus line A06 |
| I8 | LBUSA07 | Local Bus line A07 |
| I9 | LBUSC07 | Local Bus line C07 |
| I10 | LBUSA08 | Local Bus line A08 |
| I11 | LBUSC08 | Local Bus line C08 |
| I12 | LBUSA09 | Local Bus line A09 |
| I13 | LBUSC09 | Local Bus line C09 |
| I14 | LBUSA10 | Local Bus line A10 |
| I15 | LBUSC10 | Local Bus line C10 |
| I16 | LBUSA11 | Local Bus line A11 |
| I17 | LBUSC11 | Local Bus line C11 |