Model V530-EA11

Pressure Scanner Interface

**INSTRUCTION MANUAL**

March, 1998

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WARRANTY

## UNPACKING AND INSTALLATION

The Model V530 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

### Logical Address Switches

The V530 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V530 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. Refer to FIGURE 1, below.

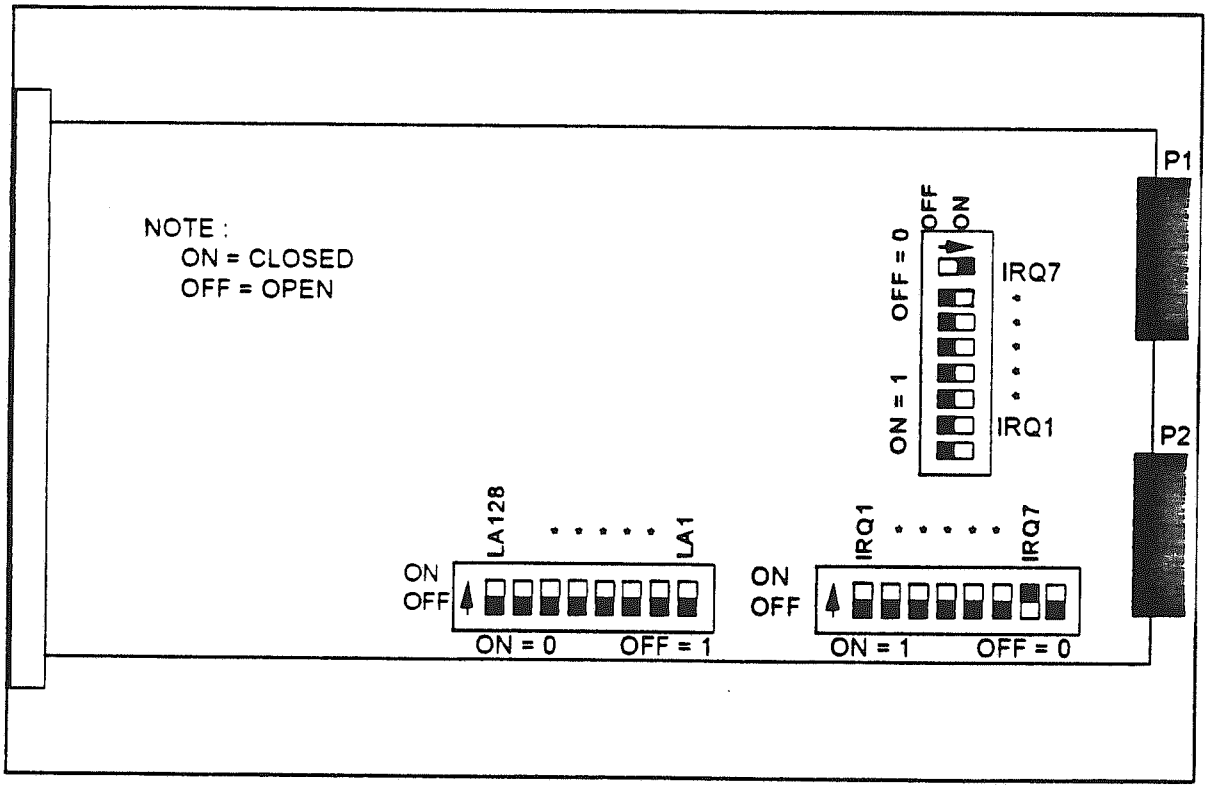


FIGURE 1 - V530 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe, pencil point, or other appropriate instrument to set the Logical Address to the desired value.

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The bit pattern for the base address is shown below:

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | LA128 | LA64 | LA32 | LA16 | LA8 | LA4 | LA2 | LA1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 15 and 14 are set to "1" (VXI defined).
Bits 13 through 6 are user-selectable via the address switches LA128-LA1.
Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

### Interrupt Switches

The V530 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 for the switch locations and switch settings. Both banks of eight-position switches must be set to the same value.

### Module Insertion

The V530 is a C-sized, single width VXIbus module. It requires 2900 milliamperes of +5 volt power, 480 milliamperes of +24 volt power, 62 milliamperes of -24 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus mainframe.

**CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE**

**WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE IN THE BACKPLANE**

## FRONT PANEL INFORMATION

### LEDs

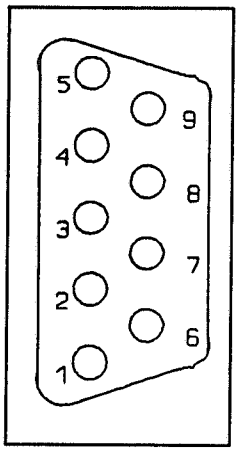
| | |
|---|---|
| ADD_REC | This LED is illuminated only when one of the operational registers (A24 offsets $12_{16}$ through $5E_{16}$, see below) is accessed. The operational registers must be enabled by setting bit #15 in the Status/Control register. |
| INT SRC | This LED turns on when scanning has stopped and the DONE Interrupt Request is enabled. |
| ACTIVE | When this LED is on, the V530 is scanning the active channels. |

## Connectors

SYNC — A single-contact LEMO is provided for initiating a scan operation. The sync input can be enabled/disabled via a board mounted jumper strap. The factory default position for this jumper is the disabled position ("A"). The top cover shield must be removed to gain access to this strap. See Figure 1 for the location of this strap.

EXT CLK — A single-contact LEMO is provided for a user-defined clock stream.

P1 — This nine-pin "D" connector receives power from the external ±18 volt power supply required with the PSI system.




| Pin # | Signal |
|---|---|
| 1 | +18 Volts |
| 2 | +18 Volts |
| 3 | Return |
| 4 | -18 Volts |
| 5 | -18 Volts |
| 6 | +18 Volts |
| 7 | Return |
| 8 | Return |
| 9 | -18 Volts |

**Figure 2 - P1 Connector Information**

P2 — This 50-socket "D" connector provides power, addressing, and control signals to the PSI pressure scanners. It also receives the analog data from the scanners. Figure 3 provides the details for this connector.

## PROGRAMMING INFORMATION

### VMEBUS/VXIBUS Addressing

Of the defined VXIbus Configuration Registers, the V530 implements those required for register-based devices. The V530 also contains a set of Operational Registers to monitor and control the functional aspects of the device. Both register sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see next page) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

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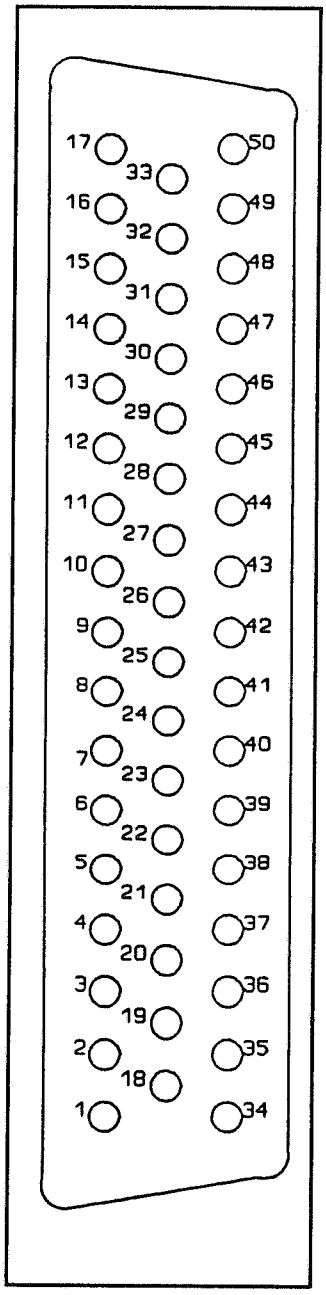



| | | | | | |
|---|---|---|---|---|---|
| 17 | +18 V | | | 50 | N/U |
| | | 33 | IFC Strobe | | |
| 16 | +18 V | | | 49 | N/U |
| | | 32 | GND | | |
| 15 | -18 V | | | 48 | PS Return |
| | | 31 | GND | | |
| 14 | -18 V | | | 47 | PS Return |
| | | 30 | IFCD7 | | |
| 13 | -18 V | | | 46 | PS Return |
| | | 29 | IFCD6 | | |
| 12 | N/U | | | 45 | CH 2 - |
| | | 28 | GND | | |
| 11 | N/U | | | 44 | CH 3 - |
| | | 27 | IFCD5 | | |
| 10 | GND | | | 43 | CH 4 - |
| | | 26 | IFCD4 | | |
| 9 | IFC Set | | | 42 | CH 1 + |
| | | 25 | IFCD3 | | |
| 8 | L6 | | | 41 | CH 1 - |
| | | 24 | GND | | |
| 7 | GND | | | 40 | CH 2 + |
| | | 23 | GND | | |
| 6 | L5 | | | 39 | CH 3 + |
| | | 22 | GND | | |
| 5 | L4 | | | 38 | CH 4 + |
| | | 21 | IFCD2 | | |
| 4 | L1 | | | 37 | GND |
| | | 20 | IFCD1 | | |
| 3 | L3 | | | 36 | GND |
| | | 19 | IFCD0 | | |
| 2 | L2 | | | 35 | GND |
| | | 18 | +18 V | | |
| 1 | L0 | | | 34 | GND |

**FIGURE 3 - CONNECTOR P2 INFORMATION**

## VXIBUS Configuration Registers

Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V530 are offset from the base address. **Note: The V530 only responds to these addresses if the Short Nonprivileged Access ($29_{16}$) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle.** Table 1 shows the applicable Configuration Registers

present in the V530, their offset from the base (Logical) address, and their Read/Write capabilities.

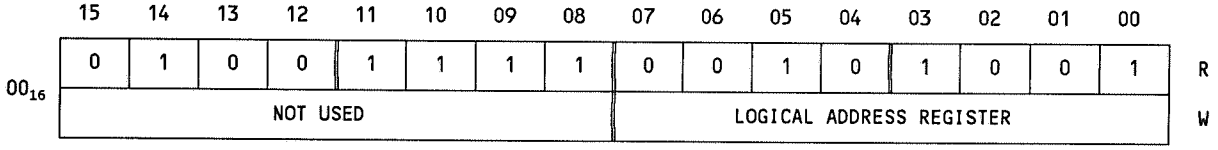
TABLE 1
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

| OFFSET | READ/WRITE CAPABILITY | REGISTER NAME |
|---|---|---|
| $00_{16}$ | READ/WRITE | ID/Logical Address Register |
| $02_{16}$ | READ ONLY | Device Type Register |
| $04_{16}$ | READ/WRITE | Status/Control Register |
| $06_{16}$ | READ/WRITE | Offset Register |
| $08_{16}$ | READ ONLY | Attribute Register |
| $1E_{16}$ | READ ONLY | Subclass Register |

The other 52 byte addresses within the Configuration Register address space are either dedicated to VXIbus Message-Based devices or are reserved for future use by the VXIbus specification, and are not used in the V530.

### ID/Logical Address Register

The format and bit assignments for the ID/Logical Address Register are as follows:




On READ transactions,

| Bit(s) | Label | Meaning |
|---|---|---|
| 15, 14 | Device Class | This is a Register-Based device. |
| 13, 12 | Address Needs | This module requires the use of A16/A24 address space. |
| 11 - 00 | Manufacturer's ID | 3881 ($F29_{16}$) for KineticSystems. |

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V530. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

### Device Type Register

The format and bit assignments for the Device Type Register are as follows:

| | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $02_{16}$ | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | R |

| Bit(s) | Label | Meaning |
|---|---|---|
| 15 - 12 | Required Memory | The V530 requires 256 bytes of additional memory space. |
| 11 - 00 | Model Code | Identifies this device as Model V530 ($530_{16}$). |

### STATUS/CONTROL REGISTER

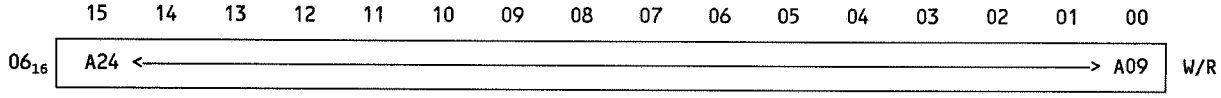
| | 15 | 14 | 13 | 12 | 11 10 09 08 07 06 05 04 | 03 | 02 | 01 | 00 | |
|---|---|---|---|---|---|---|---|---|---|---|
| $04_{16}$ | A24 ACT | MODID | S | 1 | ZEROS | RDY | PASS | 0 | RST | R |
| | A24 ENA | N/U | N/U | 1 | NOT USED | | | | RST | W |

| Bit(s) | Label | Meaning |
|---|---|---|
| 15 | A24 Enable | This bit is written with a "1" to enable A24 addressing, and reset (to "0") to disable A24 addressing. **This bit must be set to "1" to allow access to the module's Operational Registers.** Reads of this bit indicate its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET*. |
| 14 | MODID | This Read-Only bit is set to a "1" if the module is not selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line. |
| 13 | Status | This Read-Only bit indicates the status of the last operational transaction to the V530. A "1" indicates the transaction completed successfully. |
| 12 | 1 | This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1". |
| 11 - 04 | Not Used | When read, will return all "0"s. These bits are ignored when written. |
| 03 | Ready | Along with Bit 02 (Passed), this Read-Only bit will appear as a "1" to indicate its readiness to accept operational commands. |

| | | |
|---|---|---|
| 02 | Passed | See the Ready bit description. |
| 01 | Not Used | Read as "0" and ignored on write transactions. |
| 00 | Reset | This Read/Write bit controls the Soft Reset condition within the V530. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any access to the Operational Registers (see below) is inhibited. The output bit patterns from the module are maintained in the state they were in just prior to the Soft Reset being enabled. This bit can be reset by writing a "0", on power-up, or the assertion of SYSRESET*. |

## OFFSET REGISTER

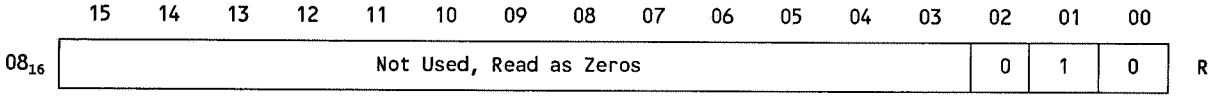
The format and bit assignments for the Offset Register are as follows:




This Read/Write register defines the base address of the V530's Operational Registers. These 16 bits contain the 16 most significant bits of the module's A24 space register addresses. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

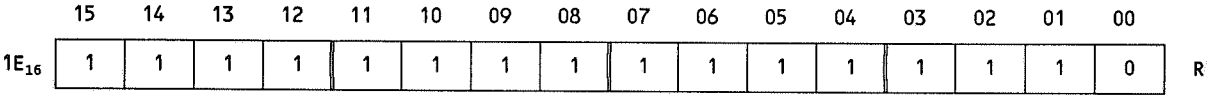
## INTERRUPT ATTRIBUTE REGISTER

The format and bit assignments for the Interrupt Attribute Register are as follows:




| Bit(s) | Label | Meaning |
|---|---|---|
| 15 - 03 | Not Used | These bits are not used by the V530, and are read as zeros. |
| 02 | Intr Control | The V530 has Interrupt Control capabilities. |
| 01 | Intr Hndlr | The V530 does not have Interrupt Handler capabilities. |
| 00 | Intr Status | The V530 has an Interrupt Status register. |

## SUBCLASS REGISTER



| Bit(s) | Label | Meaning |
|---|---|---|
| 15 | Extended Device | A "1" indicates that this is a VXIbus-defined Extended Device. |
| 14 - 00 | Register-Based | $7FFE_{16}$ indicates that this is an Extended register-based Device. |

## OPERATIONAL REGISTERS

The Operational Registers are the channels through which the functions of the V530 are controlled. For compatibility with other KineticSystems VXIbus modules in this series, these registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register. **Note: The V530 will only respond to these addresses if the Standard Nonprivileged Data Access ($39_{16}$), Standard Nonprivileged Program Access ($3A_{16}$), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for the bus cycle(s).**

Of the 256 bytes requested by the setting of the Device Type Register in the Configuration Register set, only 95 bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type register.) Table 2 shows the applicable Operational Registers present in the V530, their offset from the base (A24) address, and their Read/Write capabilities.

TABLE 2
V530 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

| A24 OFFSET | WRITE/READ MODE | REGISTER NAME |
|---|---|---|
| $00_{16}$ | WRITE/READ | Diagnostic Register |
| $02_{16}$ | READ ONLY | Interrupt Status Register |
| $12_{16}$ | READ ONLY | Converted Data Register |
| $16_{16}$ | WRITE ONLY | Converted Data Address Register |
| $1A_{16}$ | READ ONLY | Converted Data Address Register |
| $1E_{16}$ | WRITE ONLY | Scan Table Address Register |
| $22_{16}$ | READ ONLY | Scan Table Address Register |
| $26_{16}$ | WRITE ONLY | Scan Table Data Register |
| $2A_{16}$ | READ ONLY | Scan Table Data Register |
| $2E_{16}$ | WRITE ONLY | Scan Rate Register |
| $32_{16}$ | READ ONLY | Scan Rate Register |
| $36_{16}$ | READ ONLY | Single Scan |
| $3A_{16}$ | READ ONLY | Stop Scan |
| $3E_{16}$ | READ ONLY | Clear Memory Addresses |
| $42_{16}$ | READ ONLY | Enable PAM mode |
| $46_{16}$ | READ ONLY | Disable PAM mode |
| $4A_{16}$ | READ ONLY | Enable Continuous Scanning |

| A24 OFFSET | WRITE/READ MODE | REGISTER NAME |
|---|---|---|
| $4E_{16}$ | READ ONLY | Disable Continuous Scanning |
| $52_{16}$ | READ ONLY | Enable DONE INT Request |
| $56_{16}$ | READ ONLY | Disable DONE INT Request |
| $5A_{16}$ | READ ONLY | Clear DONE INT Status |
| $5E_{16}$ | READ ONLY | Test DONE INT Status |

## DIAGNOSTIC REGISTER

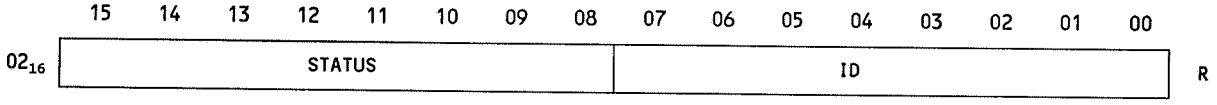
This register is included for diagnostic purposes, and is not accessed as part of writing a normal control operation. The format and bit assignments for the Diagnostic Register are as follows:

| | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $00_{16}$ | BLOCK OFFSET | | | | | | | | D | S | 0 | INT ENA | INT SRC | 0 | 0 | 0 | R |
| | DON'T CARE | | | | | | | | 0 | 0 | 0 | INT ENA | 0 | 0 | 0 | INIT | W |

| Bit | Mnemonic | Description |
|---|---|---|
| 15 - 8 | BLKOFF | Block Offset: These 8-bits contain the register offset to be accessed during a DMA (BLOCK) transfer. A value of $12_{16}$ or $1A_{16}$ would be loaded before a DMA operation is started. |
| 7 | Diagnostic | When this bit is set to a "1", the last register access to the Operational Registers (offsets $12_{16}$ through $5E_{16}$) was valid. |
| 6 | Status | When this bit is set to a "1", the last register access to the Operational Registers (offsets $12_{16}$ through $5E_{16}$) was accepted. |
| 5 | Not Used | On Read transactions, this bit returns a "0". On Write transactions, it is ignored by the module. |
| 4 | INT ENA | Interrupt Enable: setting this bit to a "1" will enable interrupts. |
| 3 | INT SRC | Interrupt Source: When this bit is set to a "1", the V530 has completed scanning. |
| 2 - 1 | Not Used | On read transactions, these bits return an all "0" pattern. On Write transactions, these bits are ignored by the module. |
| 0 | Initialize | Setting this bit to a "1" will only reset the operational registers (offsets $12_{16}$ through $5E_{16}$). The configuration registers and the Diagnostic register are unaffected. |

## INTERRUPT STATUS/ID REGISTER

This is a read only 16-bit Interrupt Status Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.




| Bit | Mnemonic | Description |
|---|---|---|
| 15 - 8 | STATUS | These eight bits will indicate a Request True or Request False condition.<br><br>Request True = $FD_{16}$<br>Request False = $FC_{16}$ |
| 7 - 0 | ID | These eight bits represent the Logical Address of the V530 Configuration Registers. |

### Converted Data Register (Offset $12_{16}$)

The Converted Data register is a read-only register that will read all 1024 pressure scanner channels. The Converted Address register will point to the first channel to be read. After each read from the Converted Data Register, the Converted Address register will increment by one. The status bit in the diagnostic register, if set to a "1", will indicate the Fresh Data flag is set. The Fresh Data flag indicates that the V530 has scanned its list of inputs, specified by the scan table, at least once and that the data is ready to be read. A "0" will indicate that all active channels have not been updated.

### Write Converted Data Address Register (Offset $16_{16}$)
### Read Converted Data Address Register (Offset $1A_{16}$)

A write to the Converted Data Address register will point to the next channel to be read by the Converted Data register. A read from this register will indicate the next channel to be read. Memory addresses zero to 1023 represent channels one to 1024. The status bit in the diagnostic register should always equal "1".

### Write Scan Table Address Register (Offset $1E_{16}$)
### Read Scan Table Address Register (Offset $22_{16}$)

A read or a write to the Scan Table Address register will point to a memory location in the Scan Table. This memory location can be read or written with new data using the Scan Table Data registers. The status bit in the diagnostic register should always equal "1".

**Write Scan Table Data Register (Offset $26_{16}$)**
**Read Scan Table Data Register (Offset $2A_{16}$)**

A write to the Scan Table Data register will select the various options for scanning different PSI systems. Refer to the section on Scan Table and Scan Table Addressing Mode on page 15 of this manual. A read will verify the contents of the Scan Table. A read or a write to the Scan Table Data register is only valid when the V530 is idle (not scanning). The status bit in the diagnostic register will equal a "1" to indicate that the V530 is idle during a read or write operation.

**Write Scan Rate Register (Offset $2E_{16}$)**
**Read Scan Rate Register (Offset $32_{16}$)**

A write to the Scan Rate register will select the various scan rate options. Refer to the section on Scan Rate Options (on page 19) for a description on the Scan Rate register layout. This register can be read to verify the contents of the Scan Rate register. A write or a read is only valid when the V530 is idle. The Diagnostic register should show the status bit set to a "1".

## CONTROL REGISTERS

The V530 has eleven control registers at offsets $36_{16}$ through $5E_{16}$. These registers are read-only and return a one-bit status code. This bit is the same as Bit 6 in the Diagnostic Register. This status code will indicate that a command was accepted, or that a test condition is true when equal to "1". These eleven control registers are described below.

### Single Scan (Offset $36_{16}$)

A read from this register will initiate a single-scan operation and clear the SCAN Done interrupt status bit. This command is accepted only when the V530 is idle (not scanning). This can be verified by the status bit in the diagnostic register. A "1" indicates the command was accepted. Note that if the V530 is strap enabled to receive an external trigger at the front panel Sync LEMO (Strap position ("B"), scanning can only be initiated by an active low TTL input at the front panel sync LEMO. The factory default setting is for external trigger disabled (Strap position ("A").

### Stop Scan (Offset $3A_{16}$)

A read from this register will stop the V530 from its current scan. The status bit in the diagnostic register, if a "1", indicates that the V530 was scanning, and the read operation was successful in stopping the scan. Once the scanning is stopped, the Converted Data Address register is initialized to "0".

### Clear Memory Address Register (Offset $3E_{16}$)

A read from this register will clear both the Converted Data and the Scan Table memory address registers to zero. This command will only be accepted when the V530 is idle. Checking the status bit in the diagnostic register, a "1" will indicate that the command was accepted.

**Enable PAM Mode (Offset $42_{16}$)**
**Disable PAM Mode (Offset $46_{16}$)**

A read of these registers will either enable or disable PAM mode. PSI scanners provide for a parallel addressing mode, referred to as PAM. More information on PAM mode can be found on page 19. Reads of these two registers will only be accepted when the V530 is idle. Checking the status bit in the diagnostic register, a "1" will indicate the command was accepted.

**Enable Continuous Scanning (Offset $4A_{16}$)**

A read of this register will enable the V530 for continuous scanning and will clear the SCAN DONE status bit. A data value of "1" indicates the command was accepted. Note that if the V530 is strap enabled to receive an external trigger at the front panel sync LEMO (Strap position "B"), scanning can only be initiated by an active low TTL input at the front panel sync LEMO. The V530 will continue to scan as long as the sync input is held low. The factory default setting is for external trigger disabled (Strap position "A").

**Disable Continuous Scanning (Offset $4E_{16}$)**

A read of this register will disable the V530 from scanning. A data value of "1" indicates the command was accepted.

**Enable DONE INT Request (Offset $52_{16}$)**
**Disable DONE INT Request (Offset $56_{16}$)**

A read of these registers will either enable or disable the SCAN DONE Interrupt Request. The SCAN DONE Interrupt Request must be enabled if the V530 is going to set an interrupt. Both registers will return a data value of "1". A data value of "1" indicates the command was accepted.

**Clear Scan DONE Status (Offset $5A_{16}$)**

A read of this register will clear the SCAN DONE status bit. A data value of "1" indicates the command was accepted.

**Test Scan DONE Status (Offset $5E_{16}$)**

A read of this register will test whether the SCAN DONE status is set or not. If data read equals "1", then SCAN DONE Status is set.

## POWER SUPPLY

In order to use the V530 with PSI pressure scanners, an external power supply must be used to provide +18 volts and -18 volts to the pressure scanners. The power supply must be capable of souring 6 amps of current at +18 volts, and 3 amps of current at -18 volts. Please refer to the PSI manual for more information on pressure scanner power budget requirements.

The ±18 volt power supply is connected to the V530 front panel via a 9-pin "D" connector. The power is then passed through the V530 to the PSI pressure scanners through the main interface

cable. A description of the V530 power supply connector is shown in Figure 2 (page 5 of this manual).

## SCANNING

The V530 provides for three types of channel scanning.

Single-scan mode is initiated by a read of the Single Scan register (offset $36_{16}$). Channels are scanned in a sequence determined by the user-defined scan table, the analog signal is digitized, and the result is stored in the converted data memory. The memory may be read at the next scan period, or as a result of SCAN DONE interrupt.

Auto-scan mode is initiated by a read of the Enable Continuous Scan register (offset $4A_{16}$). In autoscan mode, the V530 will continuously scan through the channels defined by the scan table until auto-scan is disabled by reading either the Disable Continuous Scan Register (offset $4E_{16}$) or the Stop Scan Register (offset $3A_{16}$). In autoscan mode, reading is asynchronous. The latest data for any given channel is read from the dual-ported converted data memory.

Auto-scan mode may also be controlled by an external trigger signal. The external trigger is an active-low TTL input which is received at the V530 through a front-panel LEMO connector. When the external trigger is used, the V530 will continue to scan as long as the external trigger input is held low. Scanning will stop at the end of the scan list, after the external input returns high.

## FRESH DATA FLAG

Once a scan is initiated at the V530, attempts to read the converted data will be inhibited until fresh data is available. After the V530 has completed one full pass through the scan table, it will assert the Fresh Data Flag to allow reading of the Converted Data Address register (offset $1A_{16}$).

## SCAN TABLE

The scan table is a user-defined block of memory which contains a list of all the pressure sensors to be scanned, and the order in which they will be scanned. It is contained in a 1024 word by 16-bit Scan Table memory which may be written or read. The scan table may be any length from 1 to 1024 words, with a Last Channel bit indicating the last entry in the list.

In order to create the scan table, the scan table address register is first cleared by reading the register at offset $3E_{16}$ (Clear Memory Address). Then the information for the first channel to be scanned is written to the scan table memory by writing to the register at offset $26_{16}$ (Scan Table Data). After the scan table write operation, the scan table address is automatically incremented to point to the next scan table location. The information for the next channel to be scanned is then written into the scan table memory by writing again to the Scan Table Data register. This process is repeated until the entire scan table is written to the scan table memory. The last entry in the scan table is designated by setting the Last Channel bit, bit 02, to a "1". All previous scan table entries must have bit 02 set to a "0".

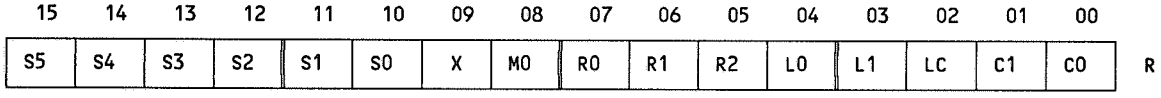
When the V530 begins scanning, it will first get the address information from the scan table memory. It will then address the appropriate pressure sensor, convert the analog input to a 16-bit digital value, and store the result in the first location of the converted data memory. It then increments the scan table memory address, gets the information for the next pressure sensor, converts the analog input, and stores the data in the next location of the converted data memory. This process will repeat until the V530 recognizes the Last Channel bit (bit 02) set to a "1" to indicate the last entry in the scan table. Once the last channel has been processed, the V530 sets the Fresh Data flag to enable reading, and either stops scanning or returns to the beginning of the scan table, depending on the scan mode selected.

## SCAN TABLE ENTRIES

The form of the V530 scan table entry depends upon the type of PSI pressure scanners being used.

### S1600-HD-RK
### S3200-RK-50

For these two I/O racks, the Scan Table Entry takes the form of an address pattern. The address is shown below:




| Bit(s) | Mnemonic | Description |
|---|---|---|
| 15 - 10 | S5 - S0 | These bits Select one of 64 possible **Sensors** within a pressure scanner module. |

| S5 | S4 | S3 | S2 | S1 | S0 | Sensor |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| . | . | . | . | . | . | . |
| . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

| | | |
|---|---|---|
| 9 | N/U | Not used, set to zero. |
| 8 | M0 | This bit selects one of two **Mulitplexer** channels within the PSI rack. |

| M0 | Mux Channel |
|---|---|
| 0 | 1 - 4 |
| 1 | 5 - 8 |

| | | |
|---|---|---|
| 7 - 5 | R2 - R0 | These bits select one of eight Racks. |

| R2 | R1 | R0 | Rack |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

| | | |
|---|---|---|
| 4 - 3 | L1 - L0 | These bits select one of four address **Latches** at the rack. |

| L1 | L0 | Latch |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

| | | |
|---|---|---|
| 2 | Last Channel | Set to a "1" to indicate the **Last Channel** in the scan list. |
| 1 - 0 | C1-C0 | These bits select one of four input **Channels** at the V530. **These bits must be set the same as L1-L0 for use with a V530.** (Note that the order of the bits is reversed.) |

| C1 | C0 | Channel |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

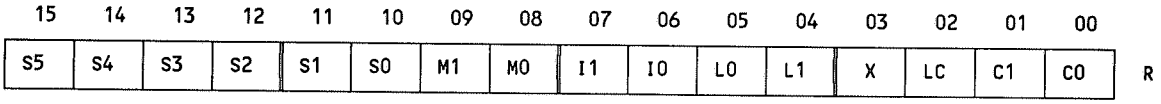
Note that M0, C1, and C0 are used together to specify a given module within the PSI rack.

| **M0** | **C1** | **C0** | **Module** |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |

For more detailed addressing information, please refer to the PSI manual.

**84-IFC**

The address pattern for the 84-IFC is shown below:




| Bit(s) | Mnemonics | Description |
|---|---|---|
| 15 - 10 | S5 - S0 | Thesse bits select one of 64 possible **Sensors** within a pressure scanner module. |

| S5 | S4 | S3 | S2 | S1 | S0 | Sensor |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| . | . | . | . | . | . | . |
| . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

| | | |
|---|---|---|
| 9 - 8 | M1 - M0 | These bits select which IFC **Mulitplexer** channel will be enabled. |

| M1 | M0 | Mux Channel |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

| | | |
|---|---|---|
| 7 - 6 | I1 - I0 | These bits select one of four **IFC** modules. |

| I1 | I0 | IFC |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

| | | |
|---|---|---|
| 5 - 4 | L1 - L0 | These bits select one of four address **Latches** at the rack. |

| L1 | L0 | Latch |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

| | | |
|---|---|---|
| 3 | N/U | Not used, set to "0". |
| 2 | LC | Set to a "1" to indicate the **Last Channel** in the scan list. |

| | | |
|---|---|---|
| 1 - 0 | C1 - C0 | These bits select one of four input **Channels** at the V530. **These bits must be set the same as L1-L0 for use with a V530.** (Note that the order of the bits is reversed.) |

| C1 | C0 | Channel |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

For more detailed addressing information, please refer to the PSI manual.

## PAM MODE

PSI scanners provide for a parallel addressing mode referred to as PAM mode. This feature is supported by the V530-EA11, and allows the user to scan at a faster rate by forcing multiple scanners to acquire pressure data in parallel. PAM mode is disabled at power-up and may be enabled by reading the register at offset $42_{16}$, Enable PAM Mode, or disabled by reading the register at offset $46_{16}$, Disable PAM Mode.

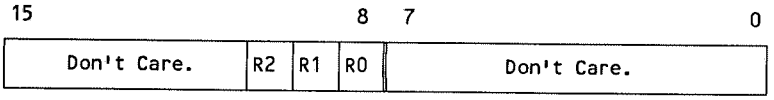
In the normal, or sequential, operating mode, the maximum scan rate is 20,000 channels per second. By using PAM mode, the maximum scan rate is increased to 50,000 channels per second. In order to use PAM mode, however, one must be careful to build a scan table that is compatible with PAM mode.

The Basic requirement in building a PAM-mode-compatible scan table is that no address latch is revisited more often than every fourth address. For an S1600-HD-RK or an S3200-RK-50, this means that a given address latch (as specified by L1 and L0) must not appear anywhere in the scan list more often than every fourth entry. For an 84-IFC, a given mulitplexer latch (as specified by L1 and L0) must not appear anywhere in the scan list more often than every fourth entry. Since L1 and L0 must match C1 and C0, as noted in the Scan Table Entry section, the above rule implies that no V530 input channel will appear in the scan table more often than every fourth entry. **Failure to follow this rule may result in incorrect data due to inadequate settling time for the analog signals.**

Please note that when the V530 is used in sequential mode, there are no restrictions on the scan table.

## SCAN RATE OPTIONS

The V530 contains a scan rate register which will allow one to select one of seven different scan rates, or an external clock. The maximum clock rate for the V530 is 1 MHz, which corresponds to a 50 kHz scan rate. The V530 will default to the maximum scan rate unless the Scan Rate Register is written (offset $2E_{16}$) with a new clock rate. The Scan Rate Register may also be read by reading the register at offset $32_{16}$. If the desired scan rate is not available on the V530, the user may supply an external TTL level clock through a front panel LEMO connector by writing the SRR with data of $0700_{16}$. The Scan Rate Register is shown below.




| R2 | R1 | R0 | Clock Rate | Scan Rate (PAM) | Scan Rate (Seq) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 MHz | 52.63 kHz | 20.41 kHz |
| 0 | 0 | 1 | 500 kHz | 26.32 kHz | 10.20 kHz |
| 0 | 1 | 0 | 250 kHz | 13.16 kHz | 5.10 kHz |
| 0 | 1 | 1 | 125 kHz | 6.58 kHz | 2.55 kHz |
| 1 | 0 | 0 | 63 kHz | 3.29 kHz | 1.28 kHz |
| 1 | 0 | 1 | 31 kHz | 1.64 kHz | 638 Hz |
| 1 | 1 | 0 | 16 kHz | 822 Hz | 319 Hz |
| 1 | 1 | 1 | External | Clock Rate/19 | Clock Rate/49 |

## BLOCK READS

To read the memory from the V530 in DMA mode, the Diagnostic and the configuration Status/Control Register must be written in the proper, order as follows:

1) For Auto-scan mode go to step 2). For Single-scan mode, wait until the V530 finishes its scan and sets the Scan Done indicator.

2) Write the Diagnostic register with a BLOCK OFFSET of $12_{16}$ to read the converted data register.

3) Read the register at offset $3E_{16}$, Clear Memory Addresses. This will set the Converted Data Memory address to zero.

4) Write the BLKENA bit to a one in the configuration Status/Control register.

   Once this bit is set, all of the operational registers are disabled except for the register at offset $12_{16}$. The value $12_{16}$ was programmed in the Block Offset section of Diagnostic register. Any access to the two kilobyte A24 address space of the V530 will only access the register pointed to by the Block Offset value stored in Diagnostic register.

5) Start the DMA reading with the register at offset $12_{16}$.

6) When all active memory is read, clear the BLKENA bit in the Configuration Status/control register. The normal group of operational registers will be enabled again.

When reading the memory with VXIbus Block mode, Address Modifier Codes $3B_{16}$ or $3F_{16}$ may be used.

## INTERRUPTS

The V530 has the ability to set an interrupt once the V530 sets SCAN DONE. SCAN DONE can be set by reading the Stop SCAN or Disable Continuous SCAN registers.

To enable the V530 for interrupts to the VXIbus, the following must be done:

Enable the DONE Interrupt Request by reading the ENA DONE INT request register.

Enable Interrupts to the VXIbus by writing Bit 4 in the Diagnostic register to a "1".

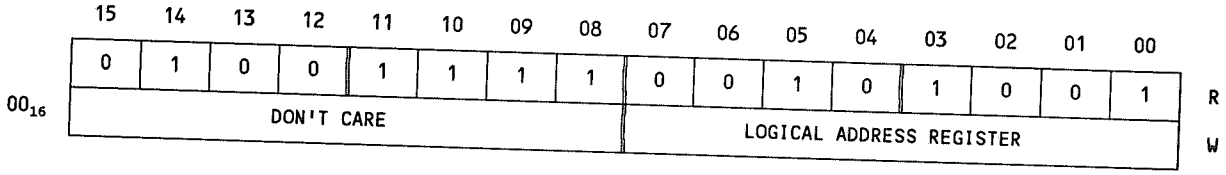
The V530 is now able to cause an interrupt on the VXIbus. Once the V530 sets an interrupt and an interrupt handler reads the Status/ID register, the Enable Interrupt bit in the Diagnostic Register is cleared automatically. Before the INT ENA bit (Bit 4 in the Diagnostic register) can be set again, check Bit 3 (INT SRC) in the Diagnostic register. If this bit is a "1", read the Clear Scan DONE Status register (Offset $5A_{16}$) to clear Bit 3 in Diagnostic register. Otherwise, false interrupts will occur.

# APPENDIX

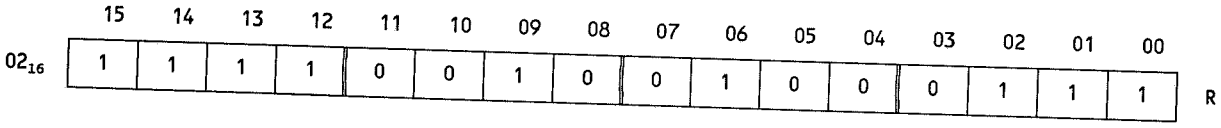
# V530 REGISTER LAYOUT

## CONFIGURATION REGISTERS

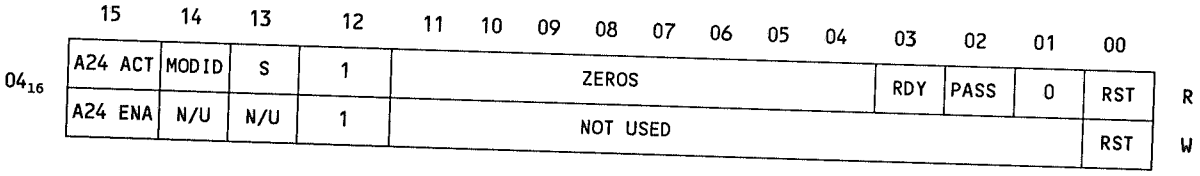
### ID/Logical Address Register



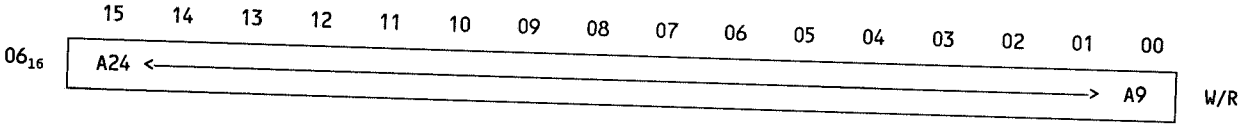

### Device Type



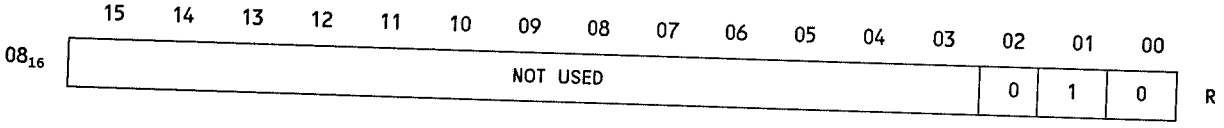

### Status/Control Register



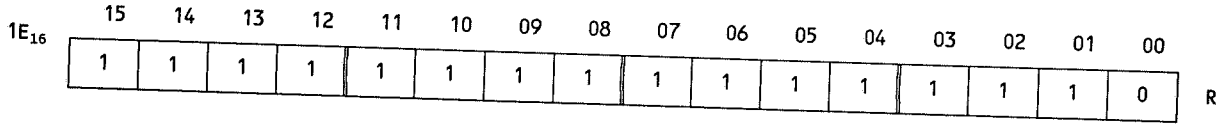

### Offset Register




### Attribute Register

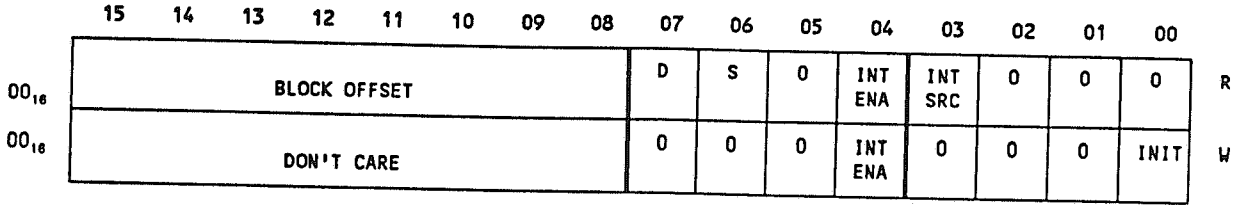



### Subclass Register

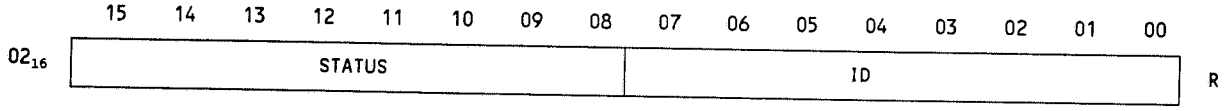


## OPERATIONAL REGISTERS

### Diagnostic Register

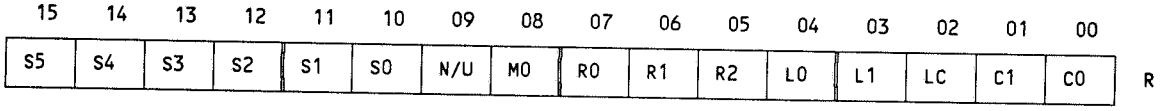



### INTERRUPT STATUS/ID REGISTER




### Scan Table Entries

**S1600-HD-RK**
**S3200-RK-50**




| S5 | S4 | S3 | S2 | S1 | S0 | Sensor |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| . | . | . | . | . | . | . |
| . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

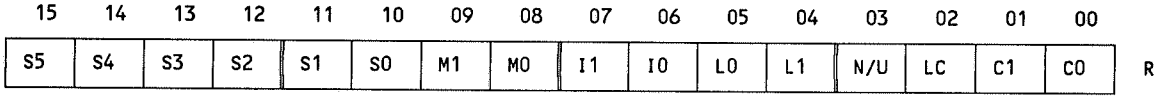
| M0 | Mux Channel |
|---|---|
| 0 | 1 - 4 |
| 1 | 5 - 8 |

| R2 | R1 | R0 | Rack |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

| L1 | L0 | Latch |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

| C1 | C0 | Channel |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

**84-IFC**




| S5 | S4 | S3 | S2 | S1 | S0 | Sensor |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| . | . | . | . | . | . | . |
| . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

| M1 | M0 | Mux Channel |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

| I1 | I0 | IFC |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

| L1 | L0 | Latch |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

| C1 | C0 | Channel |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |