Model V530-EB11

Pressure Scanner Interface

INSTRUCTION MANUAL

March, 1998

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FIGURES

TABLES

Pressure Scanner Interface

Interfaces PSI and Scanivalve analog multiplexed pressure scanners

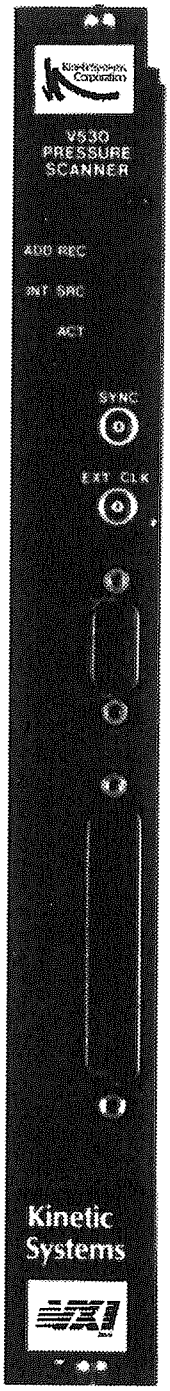
V530

Features

- **1024 channel capability with16-bit resolution**
- **Interfaces for PSI and Scanivalve pressure scanning subsystems**
- **ADC and channel control for other external multiplexed devices**
- **Internal buffer memory**
- **50,000 channel/s sample rate**

Typical Applications

- **Jet aircraft engine test cells**
- **Rocket engine test cells**
- **Wind tunnel data systems**



General Description (Product specifications and descriptions subject to change without notice.)

The V530 is a single-width, C-size, register-based, VXIbus module that provides a high-performance interface to electronic pressure scanners. Versions of the module are available for scanners from either Pressure Systems, Inc. (PSI) or Scanivalve Corporation. The V530 accepts analog signals (±2.5 V or ±5 V full scale) from the pressure scanners, and furnishes the multiplexer controls for the scanners. It contains a scan table that can be down-loaded from software. The scan table is held in a 1024 by 16-bit random access memory, allowing the V530 to monitor up to 1024 pressure channels in a user-selected order. The module also contains scan control circuitry, a multiplexer for the analog signals from the pressure scanners, a sample/hold amplifier, and a 16-bit ADC. The digital values from the ADC are loaded in a second 1024 by 16-bit RAM. The data memory is fully dual-ported so that read operations do not conflict with the conversion process.

Each V530 (in conjunction with the pressure scanners) provides an aggregate sample rate of 50,000 channels/s (128 channels in 2.56 ms or 1024 channels in 20.48 ms, for example). It can be software configured (via the scan table) to monitor any number of pressure channels up to a maximum of 1024. System performance requirements dictate the number of pressure scanning units that can be chained to a single V530. This module can be used in a single-scan or an autoscan mode. In single-scan mode, a scan can be initiated by software command. Channels selected by the Scan Table are scanned, and the Converted Data Memory is written. Reading can be accomplished at the next scan period or as the result of an interrupt. In autoscan mode, reading is totally asynchronous. The latest data for any particular channel is read from the dual-port Converted Data Memory. A gate signal applied through a front-panel mounted LEMO connector, also provides external control of the scan cycle.

When used in combination with pressure scanner interfaces, the V530 has a sample rate of 50,000 channels/s. In a 512-channel system, with one V530, one complete scan requires 10.24 ms. However, if four V530s are used, each 128-channel group is scanned in parallel, and the scan time is reduced to 2.56 ms.

The V530 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.

Scanner Supplier	Interface Type	Description
PSI	S1600-HD-RK	16 channels per S1600 module, 128 channels per rack
PSI	S3200-RK-50	32 channels per S3200 module, 192 channels per rack
PSI	84-IFC	Each interface supports 16 BP or ESP scanners
Scanivalve	ZOC12	16 or 32 channels per module; cable serviced
Scanivalve	ZOC14	16 or 32 channels per module; cable serviced
Scanivalve	ZOC16/16Px	16 channels per module; 128 channels per rack
Scanivalve	ZOC22/32Px	32 or 64 channels per module; cable serviced
Scanivalve	ZOC23/32Px	32 or 64 channels per module; cable serviced

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Item	Specification
Channel Capacity	1024 channels
Scanner Suppliers Accommodated	
Model V530-EA11	Pressure Systems, Inc.
Model V530-EB11	Scanivalve Corporation
Inputs	
Full scale input range	
Model V530-EA11	±2.5 V
Model V530-EB11	±5 V
Input protection	±17 V
Common-mode input voltage	±15 V
Common-mode rejection	-80 dB minimum; -100 dB, typical (dc to 60 Hz)
Input impedance	$2 \times 10^{12}\ \Omega$
Drift	11 µV/°C, typical
A/D Converter	
Resolution	16 bits (one part in 65,536)
Linearity error	0.003% of FSR
Differential linearity error	0.003% of FSR
Drift	±6 ppm of FSR/°C, typical
Quantization error	±½ LSB, typical
Conversion time	20 µs/channel
Front Panel Connectors	
Input signals, MUX control	50S "D"
External sync, clock	Single contact LEMO receptacle, shell size 00
Power supply (-EA11 only)	9P "D"
Mating Connectors	
Input signals, MUX control	KineticSystems Model 5935-Z1A
External sync, clock	KineticSystems Model 5910-Z1A
Power supply (-EA11 only)	KineticSystems Model 5931-Z1A

Ordering Information

Model V530-EA11 Pressure Scanner Interface for PSI Scanners
Model V530-EB11 Pressure Scanner Interface for Scanivalve Scanners

Related Products

Model 5851-Exyz Cable—50P "D" to 50S "D"
Model 5857-Axyz Cable—1-contact LEMO to Unterminated
Model 5857-Bxyz Cable—1-contact LEMO to 1-contact LEMO
Model 5857-Hxyz Cable—1-contact LEMO to BNC shielded
Model 5862-Fxyz Cable—V530 to PSI Pressure Scanner
Model 5862-Jxyz Cable—V530 to Scanivalve Pressure Scanner
Model 5910-Z1A Connector—1-contact LEMO
Model 5931-Z1A Connector—9P "D"
Model V530-0001 ±18 V Power Supply (required for PSI Scanner systems only)

UNPACKING AND INSTALLATION

The Model V530 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V530 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V530 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. Refer to FIGURE 1, below.

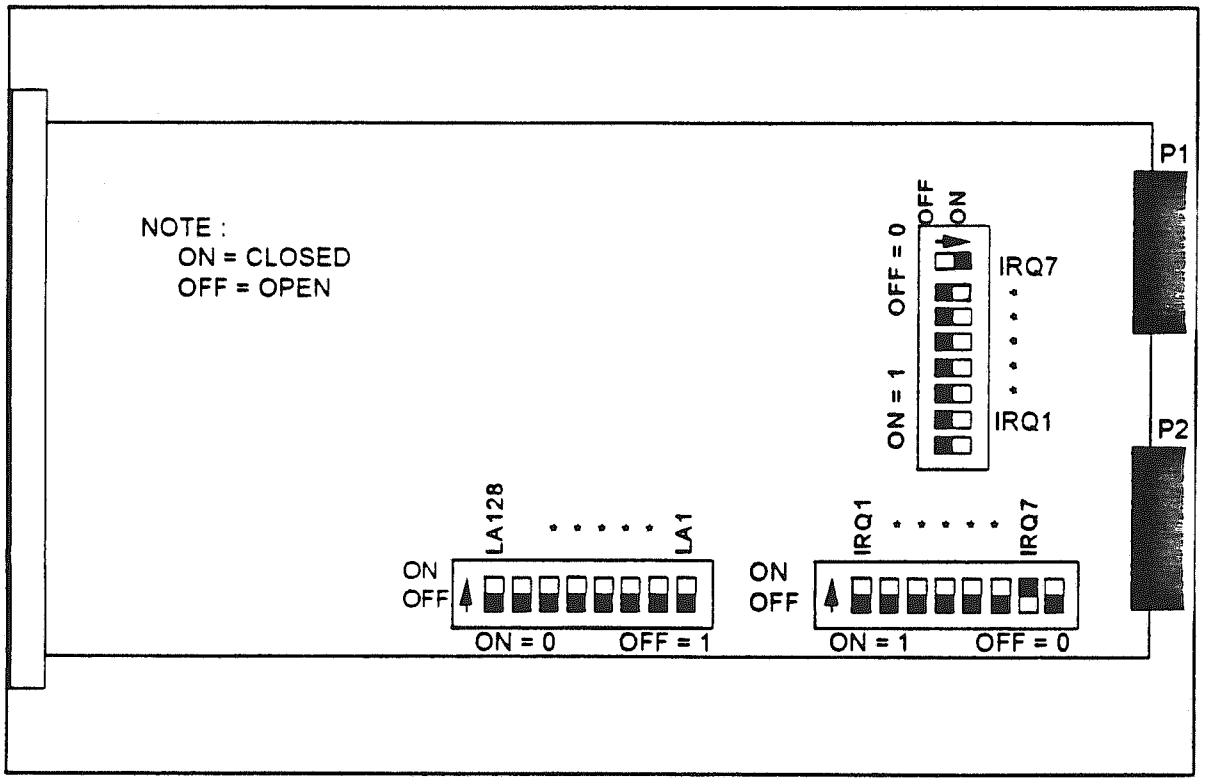


FIGURE 1 - V530 SWITCH AND STRAP LOCATIONS

The eight switches re sent a binary combination of numbers that range from zero to 255. Use a scribe, pencil point, or other appropriate instrument to set the Logical Address to the desired value.

Model V530-EB11

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0

Bits 15 and 14 are set to "1" (VXI defined).
Bits 13 through 6 are user-selectable via the address switches LA128-LA1.
Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V530 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 for the switch locations and switch settings. Both banks of eight-position switches must be set to the same value.

Module Insertion

The V530 is a C-sized, single width VXIbus module. It requires 2900 milliamperes of +5 volt power, 480 milliamperes of +24 volt power, 62 milliamperes of -24 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus mainframe.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE IN THE BACKPLANE

FRONT PANEL INFORMATION

LEDs

ADD_REC	This LED is illuminated only when one of the operational registers (offsets 12_{16} through $5E_{16}$) is accessed. The operational registers must be enabled by setting bit #15 in the Status/Control register.
ACTIVE	When this LED is on, the V530 is scanning the active channels.
INT SRC	This LED turns on when scanning has stopped and the DONE Interrupt request is enabled.

Connectors

SYNC

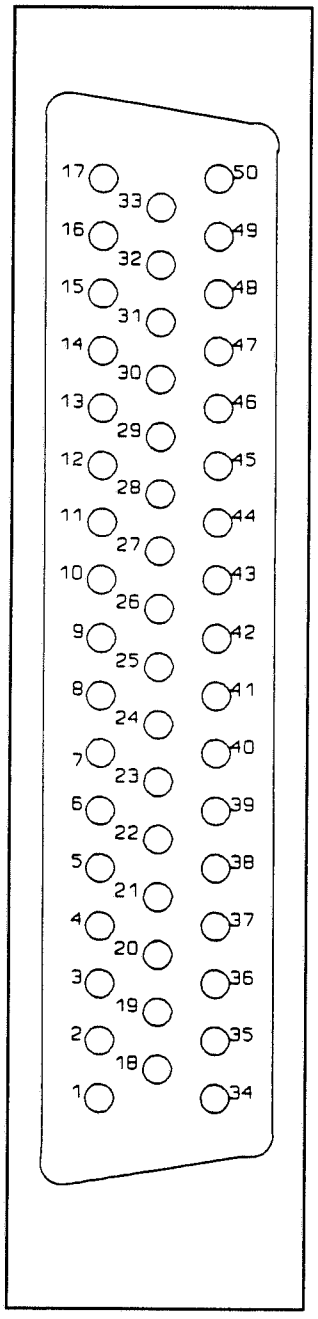
A single-contact LEMO is provided for initiating a scan operation. The sync input can be enabled/disabled via a board mounted jumper strap. The factory default position for this jumper is the disabled position. The top cover shield must be removed to gain access to this strap. See Figure 1 for the location of this strap.

EXT CLK

A single-contact LEMO is provided for a user-defined clock.

P1 & P2

These 50-contact "D" connectors provides power, addressing, and control signals to the Scanivalve pressure scanners. It also receives the analog data from the scanners. Both connectors are wired the same, allowing connection to two different racks of equipment.



17	+18 V	33	IFC Strobe	50	N/U
16	+18 V	32	GND	49	N/U
15	-18 V	31	GND	48	PS Return
14	-18 V	30	IFCD7	47	PS Return
13	-18 V	29	IFCD6	46	PS Return
12	N/U	28	GND	45	CH 2 -
11	N/U	27	IFCD5	44	CH 3 -
10	GND	26	IFCD4	43	CH 4 -
9	IFC Set	25	IFCD3	42	CH 1 +
8	L6	24	GND	41	CH 1 -
7	GND	23	GND	40	CH 2 +
6	L5	22	GND	39	CH 3 +
5	L4	21	IFCD2	38	CH 4 +
4	L1	20	IFCD1	37	GND
3	L3	19	IFCD0	36	GND
2	L2	18	+18 V	35	GND
1	L0			34	GND

FIGURE 2 - P1 & P2 CONNECTOR PINOUT

PROGRAMMING INFORMATION

VMEBUS/VXIBUS Addressing

Of the defined VXIbus Configuration Registers, the V530 implements those required for register-based devices. The V530 also contains a set of Operational Registers to monitor and control the functional aspects of the device. Both register sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see next page) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIBUS Configuration Registers

Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V530 are offset from the base address. **Note: The V530 only responds to these addresses if the Short Nonprivileged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle.** Table 1 shows the applicable Configuration Registers present in the V530, their offset from the base (Logical) address, and their Read/Write capabilities.

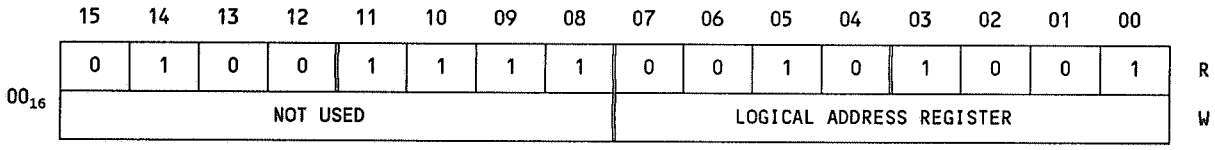
TABLE 1
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	READ/WRITE	ID/Logical Address Register
02_{16}	READ ONLY	Device Type Register
04_{16}	READ/WRITE	Status/Control Register
06_{16}	READ/WRITE	Offset Register
08_{16}	READ ONLY	Attribute Register
$1E_{16}$	READ ONLY	Subclass Register

The other 52 byte addresses within the Configuration Register address space are either dedicated to VXIbus Message-Based devices or are reserved for future use by the VXIbus specification, and are not used in the V530.

ID/Logical Address Register

The format and bit assignments for the ID/Logical Address Register are as follows:



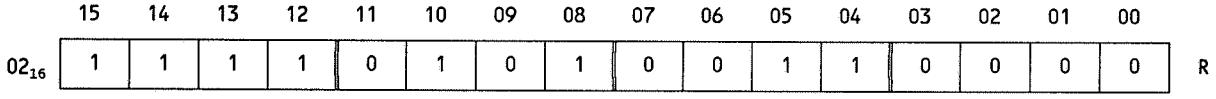
On READ transactions:

Bit(s)	Label	Meaning
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V530. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

Device Type Register

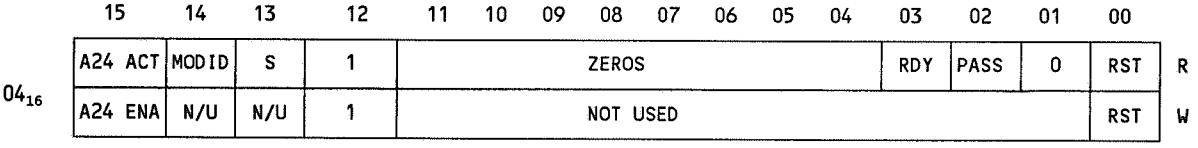
The format and bit assignments for the Device Type Register are as follows:



On READ transactions:

Bit(s)	Label	Meaning
15 - 12	Required Memory	The V530 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model V530 (530_{16}).

STATUS/CONTROL REGISTER



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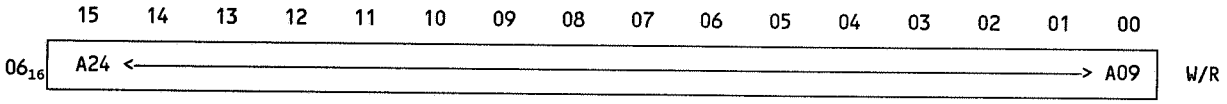
Bit(s)	Label	Meaning
15	A24 Enable	This bit is written with a "1" to enable A24 addressing and reset (to "0") to disable A24 addressing. **This bit must be set to "1" to allow access to the module's Operational Registers.** Reads of this bit indicate its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V530. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1".
11 - 04	Not Used	When read, will return all "0"s. These bits are ignored when written.
03	Ready	Along with Bit 02 (Passed), this Read-Only bit will appear as a "1" to indicate its readiness to accept operational commands.
02	Passed	See the Ready bit description.
01	Not Used	Read as "0" and ignored on write transactions.
00	Reset	This Read/Write bit controls the Soft Reset condition within the V530. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Registers (see below) is inhibited. The output bit patterns from the module are maintained in the state they were in just prior to the Soft Reset being enabled. This bit can be reset by writing a "0", on power-up, or by the assertion of SYSRESET*.

OFFSET REGISTER

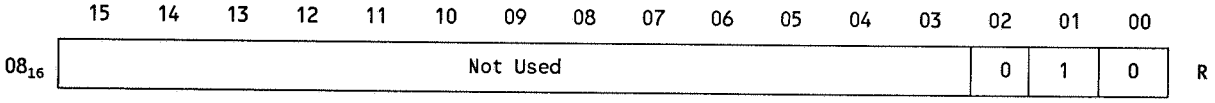
The format and bit assignments for the Offset Register are as follows:



This Read/Write register defines the base address of the V530's Operational Registers. These 16 bits contain the 16 most significant bits of the module's A24 space register addresses. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

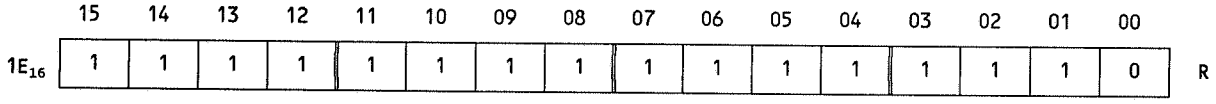
INTERRUPT ATTRIBUTE REGISTER

The format and bit assignments for the Interrupt Attribute Register are as follows:



Bit(s)	Label	Meaning
15 - 03	Not Used	These bits are not used by the V530, and are read as zeros.
02	Intr Control	The V530 does have Interrupt Control capabilities.
01	Intr Handler	The V530 does not have Interrupt Handler capabilities.
00	Intr Status	The V530 does have an Interrupt Status register.

SUBCLASS REGISTER



Bit(s)	Label	Meaning
15	Extended Device	A "1" indicates that this is a VXIbus-defined Extended Device.
14 - 00	Register-Based	$7FFE_{16}$ indicates that this is an Extended register-based Device.

OPERATIONAL REGISTERS

The Operational Registers are the channels through which the functions of the V530 are controlled. For compatibility with other KineticSystems VXIbus modules in this series, these

registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register. **Note: The V530 will only respond to these addresses if the Standard Nonprivileged Data Access (39_{16}), Standard Nonprivileged Program Access ($3A_{16}$), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for the bus cycle(s).**

Of the 256 bytes requested by the setting of the Device Type Register in the Configuration Register set, only 44 bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type register.) Table 2 shows the applicable Operational Registers present in the V530, their offset from the base (A24) address, and their Read/Write capabilities.

TABLE 2
V530 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

A24 OFFSET	WRITE/READ MODE	REGISTER NAME
00_{16}	WRITE/READ	Diagnostic Register
02_{16}	READ ONLY	Interrupt Status Register
12_{16}	READ ONLY	Converted Data Register
16_{16}	WRITE ONLY	Converted Data Address Register
$1A_{16}$	READ ONLY	Converted Data Address Register
$1E_{16}$	WRITE ONLY	Scan Table Address Register
22_{16}	READ ONLY	Scan Table Address Register
26_{16}	WRITE ONLY	Scan Table Data Register
$2A_{16}$	READ ONLY	Scan Table Data Register
$2E_{16}$	WRITE ONLY	Scan Rate Register
32_{16}	READ ONLY	Scan Rate Register
36_{16}	READ ONLY	Single Scan
$3A_{16}$	READ ONLY	Stop Scan
$3E_{16}$	READ ONLY	Clear Memory Addresses
42_{16}	READ ONLY	Enable Ring mode
46_{16}	READ ONLY	Disable Ring mode
$4A_{16}$	READ ONLY	Enable Continuous Scanning
$4E_{16}$	READ ONLY	Disable Continuous Scanning
52_{16}	READ ONLY	Enable DONE INT Request
56_{16}	READ ONLY	Disable DONE INT Request
$5A_{16}$	READ ONLY	Clear DONE INT Status
$5E_{16}$	READ ONLY	Test DONE INT Status

DIAGNOSTIC REGISTER

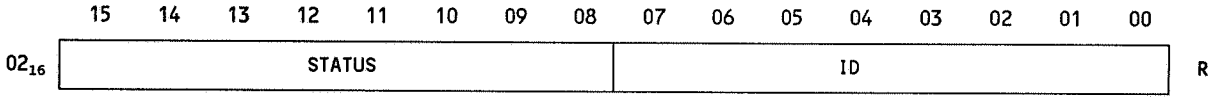
This register is included for diagnostic purposes, and is not accessed as part of a normal control operation. The format and bit assignments for the Diagnostic Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	BLOCK OFFSET								D	S	0	INT ENA	INT SRC	0	0	0	R
	DON'T CARE								0	0	0	INT ENA	0	0	0	INIT	W

Bit	Mnemonic	Description
15 - 8	BLKOFF	Block Offset; These 8-bits contain the register offset to be accessed during a DMA (BLOCK) transfer. A value of 12_{16} or $1A_{16}$ should be loaded before a DMA operation is started.
7	Diagnostic	When this bit is set to a "1", the last register access to the Operational Registers (offsets 12_{16} through $5E_{16}$) was valid.
6	Status	When this bit is set to a "1", the last register access to the Operational Registers (offsets 12_{16} through $5E_{16}$) was accepted.
5	Not Used	On Read transactions, this bit returns a "0". On Write transactions, it is ignored by the module.
4	INT ENA	Interrupt Enable; setting this bit to a "1" will enable interrupts.
3	INT SRC	Interrupt Source; When this bit is set to a "1", the V530 is done scanning.
2 - 1	Not Used	On read transactions, these bits return an all "0" pattern. On Write transactions, these bits are ignored by the module.
0	Initialize	Setting this bit to a "1" will reset the operational registers (offsets 12_{16} through $5E_{16}$). The configuration registers and the Diagnostic register are unaffected.

INTERRUPT STATUS/ID REGISTER

This is a read only 16-bit Interrupt Status Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.



Bit	Mnemonic	Description
15 - 8	STATUS	These eight bits will indicate a Request True or Request False. Request True = FD_{16} Request False = FC_{16}
7-0	ID	These eight bits represent the Logical Address of the V530 Configuration Registers.

Converted Data Register (Offset 12_{16})

The Converted Data register is a read-only register through whjich one can read all 1024 input channels. The Converted Address register (see below) will point to the first channel to be read through the Converted Data Register. After each read, the Converted Address register will increment by one. The status bit in the diagnostic register, if set to a "1", indicates that the Fresh Data flag is set. The Fresh Data flag indicates the V530 scanned its list of inputs, specified by the scan table, at least once since the last read operation, and the data is ready to be read. A "0" will indicate that all active channels have not be updated.

Write Converted Data Address Register (Offset 16_{16})
Read Converted Data Address Register (Offset $1A_{16}$)

A write to the Converted Data Address register will point to the next channel to be read by the Converted Data register. A read from this register will indicate the next channel to be read. Memory addresses zero to 1023 represent channels one to 1024. The status bit in the diagnostic register should always equal "1" after a write or read to this register.

Write Scan Table Address Register (Offset $1E_{16}$)
Read Scan Table Address Register (Offset 22_{16})

A read or a write to the Scan Table Address register will point to a memory location in the Scan Table. This memory location can then be read or written with new data using the Scan Table Data registers. The status bit in the diagnostic register should always equal "1".

Write Scan Table Data Register (Offset 26_{16})
Read Scan Table Data Register (Offset $2A_{16}$)

A write to the Scan Table Data register will select the various options for scanning different Scanivalve systems. Refer to the sections on the Scan Table and Scan Table Addressing Modes on pages 15 and 16 of this manual. A read of the Scan Table Data register will verify the contents of the Scan Table. A read or a write to the Scan Table Data register is only valid when the V530 is idle (not scanning). The status bit in the diagnostic register will equal a "1" to indicate the V530 is idle during a read or write operation.

Write Scan Rate Register (Offset $2E_{16}$)
Read Scan Rate Register (Offset 32_{16})

A write to the Scan Rate register will select a scan rate option. Refer to the section on Scan Rate Options (page 17) for a description on the Scan Rate register. This register can be read to verify the contents. A write or a read is only valid when the V530 is idle. Checking the Diagnostic register, the status bit should equal a "1".

CONTROL REGISTERS

The V530 has eleven control registers at offsets 36_{16} through $5E_{16}$. These registers are read-only and return a one-bit status code. This bit has the same meaning as Bit 6 in the Diagnostic Register. This status code will indicate the command was accepted or a test condition is true when equal to "1". These eleven control registers are described below:

Single Scan (Offset 36_{16})

A read from this register will initiate a single scan operation and clear the SCAN Done interrupt status bit. This command is accepted only when the V530 is idle (not scanning). This can be verified by the status bit in the diagnostic register. A "1" indicates the command was accepted. Note that if the V530 is strap enabled to receive an external trigger at the front panel sync LEMO, scanning can only be initiated by an active low TTL input at the front panel sync LEMO. The factory default setting is for external trigger disabled.

Stop Scan (Offset $3A_{16}$)

A read from this register will stop the V530 from its current scan. The status bit in the diagnostic register, if a "1", indicates that the V530 was scanning and a read from the register at offset $3A_{16}$ was successful in stopping the scan. Once the scanning is stopped, the Converted Data Address register is initialized to "0".

Clear Memory Address Register (Offset $3E_{16}$)

A read from this register will clear both the Converted Data and the Scan Table memory address registers to "0". This command will only be accepted when the V530 is idle. Checking the status bit in the diagnostic register, a "1" will indicate the command was accepted.

Enable Ring Mode (Offset 42_{16})
Disable Ring Mode (Offset 46_{16})

A read from these registers will either enable or disable Ring mode. Scanivalve scanners provide for a parallel addressing mode referred to as Ring mode. More information on Ring mode can be found on page 17. These two registers will only be accessed when the V530 is idle. Checking the status bit in the diagnostic register, a "1" will indicate the command was accepted.

Enable Continuous Scanning (Offset $4A_{16}$)

A read from this register will enable the V530 for continuous scanning, and it will clear the SCAN DONE status bit. A data value of "1" indicates the command was accepted. Note that if the V530 is strap enabled to receive an external trigger at the front panel sync LEMO, scanning can only be initiated by an active low TTL input at the front panel sync LEMO. The V530 will continue to scan as long as the sync input is held low. The factory default setting is for external trigger disabled.

Disable Continuous Scanning (Offset $4E_{16}$)

A read from this register will disable the V530 from scanning. A data value of "1" indicates the command was accepted.

Enable DONE INT Request (Offset 52_{16})
Disable DONE INT Request (Offset 56_{16})

A read from these registers will either enable or disable the SCAN DONE Interrupt Request. The SCAN DONE Interrupt Request must be enabled if the V530 is going to generate an interrupt. Both registers will return a data value of "1", indicating that the command was accepted.

Clear Scan DONE Status (Offset $5A_{16}$)

A read from this register will clear the SCAN DONE status bit. A data value of "1" indicates the command was accepted.

Test Scan DONE Status (Offset $5E_{16}$)

A read from this register will test whether the SCAN DONE status is set or not. If read data equals "1", then the SCAN DONE Status is set.

SCANNING

The V530 provides for two types of channel scanning: single-scan, and Auto-scan.

Single-scan mode is initiated by a read from the Single Scan register (offset 36_{16}). Channels are scanned in a sequence determined by the user-defined scan table, the analog signal is digitized, and the result is stored in the converted data memory. The memory may be read at the next scan period or as a result of a SCAN DONE interrupt.

Auto-scan mode is initiated by a read from Enable Continuous Scan register (offset $4A_{16}$). In autoscan mode, the V530 will continuously scan through the channels defined by the scan table, until auto-scan is disabled by reading either the Disable Continuous Scan Register (offset $4E_{16}$) or the Stop Scan Register (offset $3A_{16}$). In autoscan mode, reading is asynchronous. The latest data for any given channel is read from the dual-ported converted data memory.

Auto-scan mode may also be controlled by an external trigger signal. The external trigger is an active-low TTL input which is received at the V530 through a front panel LEMO connector. When the external trigger is used, the V530 will continue to scan as long as the external trigger input is **held low**. Scanning will stop, at the <u>end</u> of the scan list, after the external input returns to a high state.

FRESH DATA FLAG

Once a scan is initiated at the V530, attempts to read the converted data will be inhibited until fresh data is available. After the V530 has completed one full pass through the scan table, it will assert the Fresh Data Flag to allow reading of the Converted Data Address register (offset $1A_{16}$).

SCAN TABLE

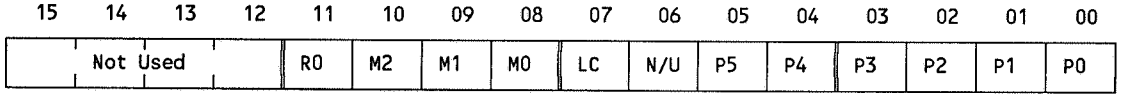
The scan table is a user-defined block of memory which contains a list of all the pressure sensors to be scanned and the order in which they will be scanned. It is contained in a 1024 word by 16-bit Scan Table memory which may be written or read. The scan table may be any length from 1 to 1024 words, with a Last Channel bit indicating the last entry in the list.

In order to create the scan table, the scan table address register is first cleared by reading the register at offset $3E_{16}$ (Clear Memory Address register). Then the information for the first channel to be scanned is written to the scan table memory by writing to the register at offset 26_{16} (Scan Table Data register). After the scan table write operation, the scan table address is automatically incremented to point to the next scan table location. The information for the next channel to be scanned is then written into the scan table memory by writing to the register at offset 26_{16} (Scan Table Data register). This process is repeated until the entire scan table is written to memory. The last entry in the scan table is designated by setting the Last Channel bit, bit 02, to a "1". All previous scan table entries must have bit 02 set to a "0".

When the V530 begins scanning, it will first get the address information from the scan table memory. It will then address the appropriate pressure sensor, convert the analog input to a 16-bit digital value, and store the result in the first location of the converted data memory. It then increments the scan table memory address, gets the information for the next pressure sensor, converts the analog input, and stores the data in the next location of the converted data memory. This process will repeat until the V530 recognizes the Last Channel bit (bit 02) set to a "1" to indicate the last entry in the scan table. Once the last channel has been processed, the V530 sets the Fresh Data flag to enable reading, and either stops scanning or returns to the beginning of the scan table, depending on the scan mode.

SCAN TABLE ADDRESSING

The address pattern used in the V530-EB11 is shown below:



Bit	Mnemonics	Description
15 - 12	X	Reserved bits; set to "0"s.
11	R0	Selects one of two Racks.

R0	Rack
0	0
1	1

Bit	Mnemonics	Description
10 - 8	M2 - M0	Select one of eight modules in a rack.

M2	M1	M0	Module
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

7	LC	Set to a "1" to indicate the Last Channel in the scan list.
6	X	Reserved bit; set to zero
5 - 0	P5-P0	Select one of 64 possible **Sensors** within a pressure scanner module.

P5	P4	P3	P2	P1	P0	Sensor
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	1	63

RING MODE

Scanivalve scanners provide for a parallel addressing mode referred to as RING mode. This feature is supported by the V530-EA11 and allows the user to scan at a faster rate by forcing multiple scanners to acquire pressure data in parallel. RING mode is disabled at power-up, and may be enabled by reading the register at offset 42_{16} (Enable RING mode) or disabled by reading the register at offset 46_{16} (Disable RING mode).

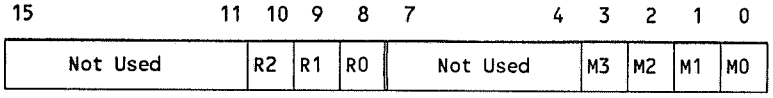
In the normal, or sequential, operating mode, the maximum scan rate is 20,000 channels per second. By using RING mode, the maximum scan rate is increased to 50,000 channels per second. In order to use RING mode, however, the user must be careful to build a scan table that is compatible with RING mode.

The basic requirement in building a RING-mode-compatible scan table is that no module be revisited more often than the ring mode register allows. For a given ring size, N, in the ring mode register, no module may appear in the scan table more often than every Nth entry. **Failure to follow this rule may result in incorrect data due to inadequate settling time for the analog signals.**

Please note that when the V530 is used in sequential mode there are no restrictions on the scan table.

SCAN RATE RING SIZE OPTIONS

The V530 contains a scan rate/ring mode register which will allow the user to select one of seven different scan rates, or an external clock. The maximum clock rate for the V530 is 1 MHz, which corresponds to a 50 kHz scan rate. The V530 will default to the maximum scan rate unless the Scan Rate register is written (the register at offset $2E_{16}$). The Scan Rate register may also be read by reading the register at offset 32_{16}). If the desired scan rate is not available on the V530, the user may supply an external TTL level clock through a front panel LEMO connector — by writing the Scan Rate register with data of 0700_{16}. The Scan Rate register, and a description of the bits is as follows:



R2	R1	R0	Clock Rate	Scan Rate (PAM)	Scan Rate (Seq)
0	0	0	1 MHz	52.63 kHz	20.41 kHz
0	0	1	500 kHz	26.32 kHz	10.20 kHz
0	1	0	250 kHz	13.16 kHz	5.10 kHz
0	1	1	125 kHz	6.58 kHz	2.55 kHz
1	0	0	63 kHz	3.29 kHz	1.28 kHz
1	0	1	31 kHz	1.64 kHz	638 Hz
1	1	0	16 kHz	822 Hz	319 Hz
1	1	1	External	Clock Rate/19	Clock Rate/49

The ring mode bits, M3 - M0, define the number of modules that will be addressed in parallel, referred to as the ring size. The minimum ring size allowed is three, and the optimum size is eight. Creating a ring larger than eight modules will cause an unnecessary delay at the beginning of the scan loop. Note that the ring mode bits, M3 - M0, are ignored while scanning in sequencial mode.

M3	M2	M1	M0	Ring Size
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
.	.	.	.	.
.	.	.	.	.
1	1	1	1	63

BLOCK READS

To read the memory from the V530 in DMA mode, the Diagnostic and the configuration Status/Control Register must be written in the proper order, as follows:

1) For Auto-scan mode go to next step. For Single-scan, wait for the V530 to finish its current scan and set the Scan Done status.

2) Write the Diagnostic register (offset 00_{16} within the Operational Register set) with the BLOCK OFFSET of 12_{16} to read the Converted Data Register.

3) Read the register at offset $3E_{16}$ (Clear Memory Addresses). This will set the Converted Data Memory address to zero.

4) Write the BLKENA bit, setting it to a "1" in the configuration Status/Control register.

   Once this bit is set, all of the operational registers are disabled, except for the register at offset 12_{16}. The value 12_{16} was programmed in the Block Offset section of Diagnostic register. Any access to the two kilobyte A24 address space of the V530 will only access the Block Offset value stored in Diagnostic register.

5) Start the DMA reads at the operational register offset 12_{16}.

6) When all active memory is read, clear the BLKENA bit in the Configuration Status/Control register. The normal operational registers will be enabled again.

VXIbus Block mode may be used to read the memory using Address Modifier Code $3B_{16}$ and $3F_{16}$.

INTERRUPTS

The V530 has the ability to set an interrupt once the V530 sets SCAN DONE. SCAN DONE is set by reading the Stop SCAN register or the Disable Continuous SCAN register.

To enable the V530 to interrupt the VXIbus, the following must be done:

Enable the DONE Interrupt Request by reading the ENA DONE INT REQ register.

Enable Interrupts to the VXIbus by writing Bit 4 in the Diagnostic register to a "1".

The V530 is now able to cause an interrupt on the VXIbus. Once the V530 sets an interrupt and an interrupt handler reads the Status/ID register, the Enable Interrupt bit in the Diagnostic Register is cleared automatically. Before the INT ENA Bit (bit 4 in the Diagnostic register) can be set again, check Bit 3, INT SRC of the Diagnostic register. If this bit is a one, read the Clear DONE INT status register (offset $5A_{16}$) to clear Bit 3 in Diagnostic register. Otherwise false interrupts will occur.

APPENDIX

V530 REGISTER LAYOUT

CONFIGURATION REGISTERS

ID/Logical Address Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1	R
	DON'T CARE								LOGICAL ADDRESS REGISTER								W

Device Type

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	1	1	1	1	0	0	1	0	0	1	0	0	0	1	1	1	R

Status/Control Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
04_{16}	A24 ACT	MODID	S	1	ZEROS								RDY	PASS	0	RST	R
	A24 ENA	N/U	N/U	1	NOT USED											RST	W

Offset Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
06_{16}	A24 <----------															A9	W/R

Attribute Register

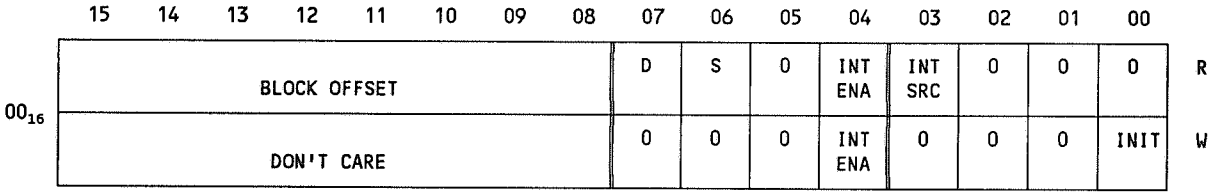
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
08_{16}	NOT USED													0	1	0	R

Subclass Register

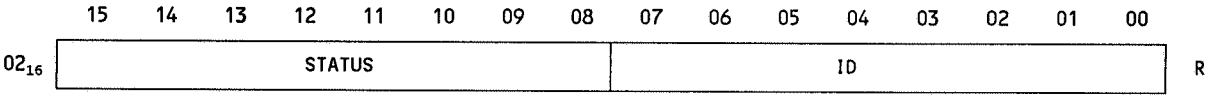
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	R

OPERATIONAL REGISTERS

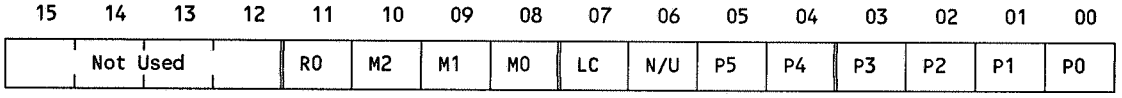
Diagnostic Register



INTERRUPT STATUS/ID REGISTER



Scan Table Entries

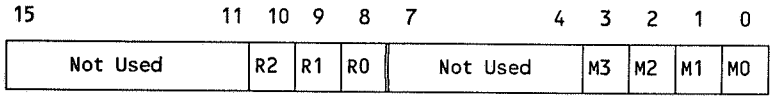


R0	Rack
0	0
1	1

M2	M1	M0	Module
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

P5	P4	P3	P2	P1	P0	Sensor
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	1	63

Scan Rate Register



R2	R1	R0	Clock Rate	Scan Rate (PAM)	Scan Rate (Seq)
0	0	0	1 MHz	52.63 kHz	20.41 kHz
0	0	1	500 kHz	26.32 kHz	10.20 kHz
0	1	0	250 kHz	13.16 kHz	5.10 kHz
0	1	1	125 kHz	6.58 kHz	2.55 kHz
1	0	0	63 kHz	3.29 kHz	1.28 kHz
1	0	1	31 kHz	1.64 kHz	638 Hz
1	1	0	16 kHz	822 Hz	319 Hz
1	1	1	External	Clock Rate/19	Clock Rate/49

M3	M2	M1	M0	Ring Size
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
.	.	.	.	.
.	.	.	.	.
1	1	1	1	63