Model V605-MA11/NA11

6-Channel, 2.5 MHz Optically-
Isolated Counter

INSTRUCTION MANUAL

April, 1998

*****Special Option*****

Model V605-S001

6-channel 2.5 MHz Optically-Isolated Counter

December, 1994

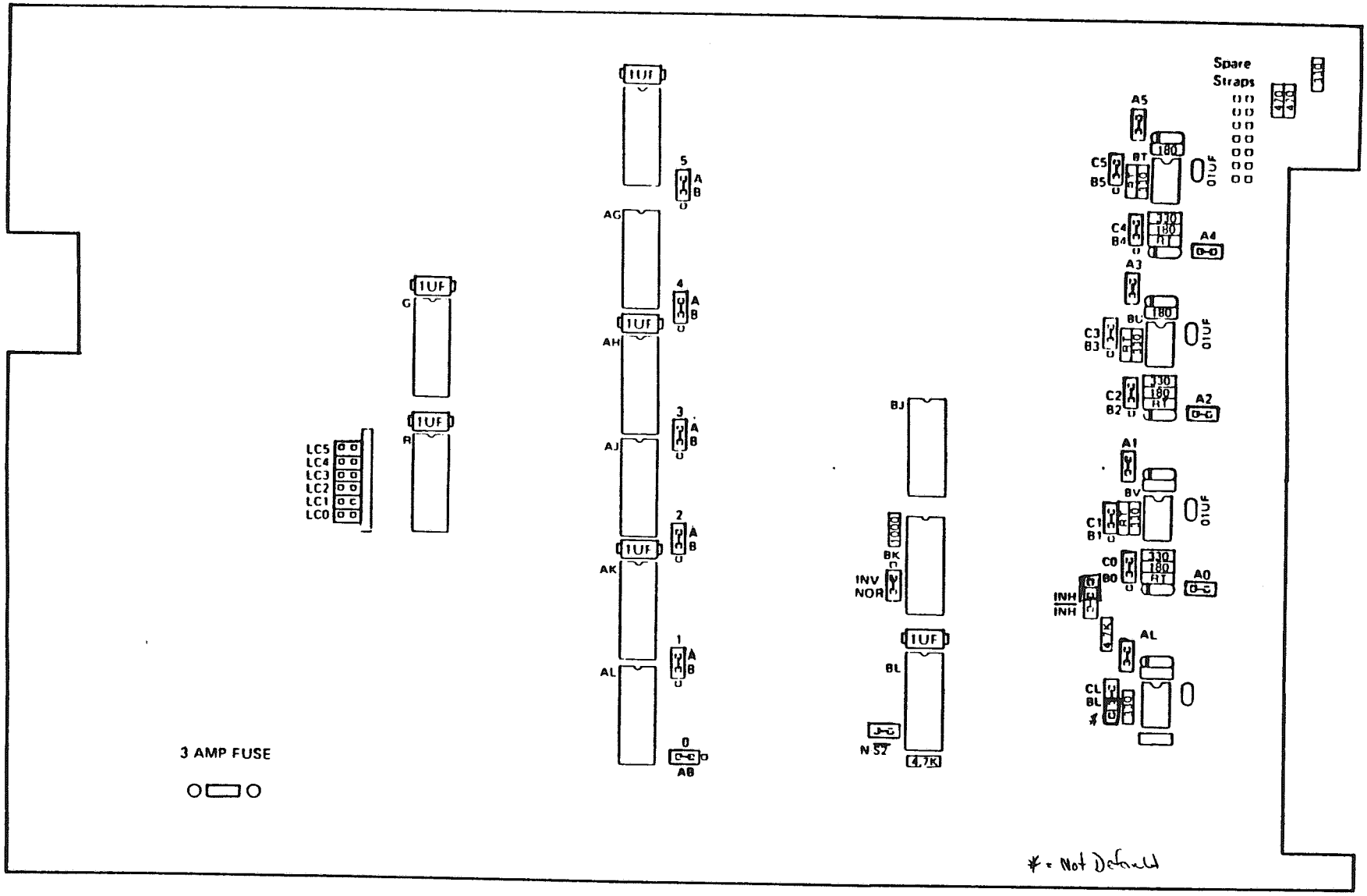
*****Special Option*****

Model V605-S001

The Model V605-S001 is the same as the V605-MA11 except jumpers have been preconfigured per customer specifications.

LC0-LC5	Strapped as default (default)
0-5	Strapped in the A position (default)
$\overline{\text{N.S2}}$	Strapped (default)
INV/NOR	Strapped Nor (default)
A0-A5	Strapped (default)
B0/C0-B5/C5	Strapped C0-C5 (default)
Al	Strapped (default)
B1-C1	Strapped BL (Not defaault)
INH/$\overline{\text{INH}}$	Set to INH (Not default)

December, 1994
PTS


Spare
Straps
1UF
5
AG
4
AH
3
AJ
2
AK
1
AL
0
AB
G
R
LC5
LC4
LC3
LC2
LC1
LC0
BJ
BK
INV
NOR
BL
N ST
4.7K
A5
C5
B5
A4
C4
B4
A3
C3
B3
A2
C2
B2
A1
C1
B1
A0
C0
B0
INH
INH
AL
CL
BL
.01UF
180
330
3 AMP FUSE
* = Not Default

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WARRANTY
NPD

6-channel, Optically Isolated Counter

Each channel counts from dc to 2.5 MHz with ground isolation

V605

Features

- **Six counters**
- **Maximum count of 24 bits (16,777,215) on each channel**
- **Optically isolated inputs**
- **Counter-inhibit input**
- **External isolated latch signal to update output registers**
- **Interrupt on overflow**
- **dc to 2.5 MHz count rate**

Typical Applications

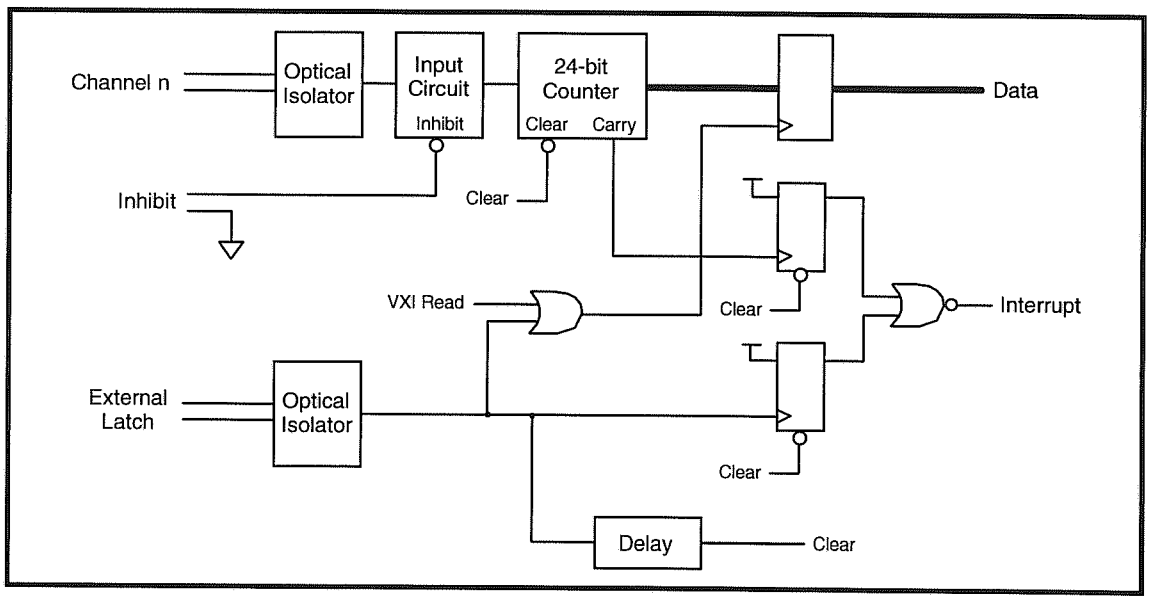
- **Test cells**
- **Nuclear accelerators**
- **Applications with high ground noise**

General Description *(Product specifications and descriptions subject to change without notice.)*

The V605 is a single-width, C-size, register-based, VXIbus module that contains six 24-bit, optically isolated counters. A signal in the range of +2.4 V to +5 V, with a 5 mA drive capability, is required to turn the optical isolator on. All inputs accept this as a logical "one" and clock the counter chains on the zero-to-one transition. The minimum clock pulse width is 100 ns. Counting can be suppressed by the application of a low-true, TTL-level signal at the front-panel Inhibit input.

Each counter's value must be loaded into its output register before it can be read by software. Upon receipt of an external Latch signal at the module's front panel, all six output registers are updated with the current contents of the counters. The output registers will not change until another Latch signal is received. The six counting chains, however, will continue to be incremented at rates determined by the incoming clock signals. The Latch input circuit has the same characteristics as the counter inputs, except it is not affected by the Inhibit input.

The V605 can generate an interrupt either on the receipt of an external Latch signal, or on the overflow of any one of the six counter chains. Separate Interrupt Enable commands are provided, and an Interrupt Status Register can be read to determine the exact source of the interrupt. The Interrupt Source bits are cleared by software commands. The V605 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.



Item	Specification
Number of Channels	6, optically isolated
Input Voltage Levels	
Logic "0"	0.0 V to 0.8 V
Logic "1"	2.4 V to 5.0 V
Input Current Requirements	5 mA
Counter/Latch Inputs	
Input-output insulation	1µA, with 45% relative humidity, t = 5s, V_{I-O} = 3 kV dc, T_A = 25°C
Input-output resistance	10^{12} Ω
Maximum Clock Rate (per channel)	2.5 MHz
Input Connector Types	
Counter/latch connectors	2-pin LEMO receptacle, shell size 0
Inhibit connector	Single-pin LEMO receptacle, shell size 00
Mating Connectors	
Counter/latch connectors	KineticSystems Model 5911-Z1A
Inhibit connector	KineticSystems Model 5910-Z1A
Power Requirements	
+5 V	2.6 A, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-sized VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V605-MA11 6-channel, 2.5 MHz Optically-Isolated Counter

Related Products

Model 5857-Axyz Cable—1-contact LEMO to Unterminated
Model 5857-Bxyz Cable—1-contact LEMO to 1-contact LEMO
Model 5857-Cxyz Cable—2-contact LEMO to Unterminated
Model 5857-Dxyz Cable—2-contact LEMO to 2-contact LEMO
Model 5857-Gxyz Cable—2-contact LEMO to BNC shielded
Model 5857-Hxyz Cable—1-contact LEMO to BNC shielded
Model 5910-Z1A Connector—1-contact LEMO
Model 5911-Z1A Connector—2-contact LEMO

UNPACKING AND INSTALLATION

The Model V605 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V605 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device.) The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V605 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the modules right-side ground shield. Refer to FIGURE 1 below.

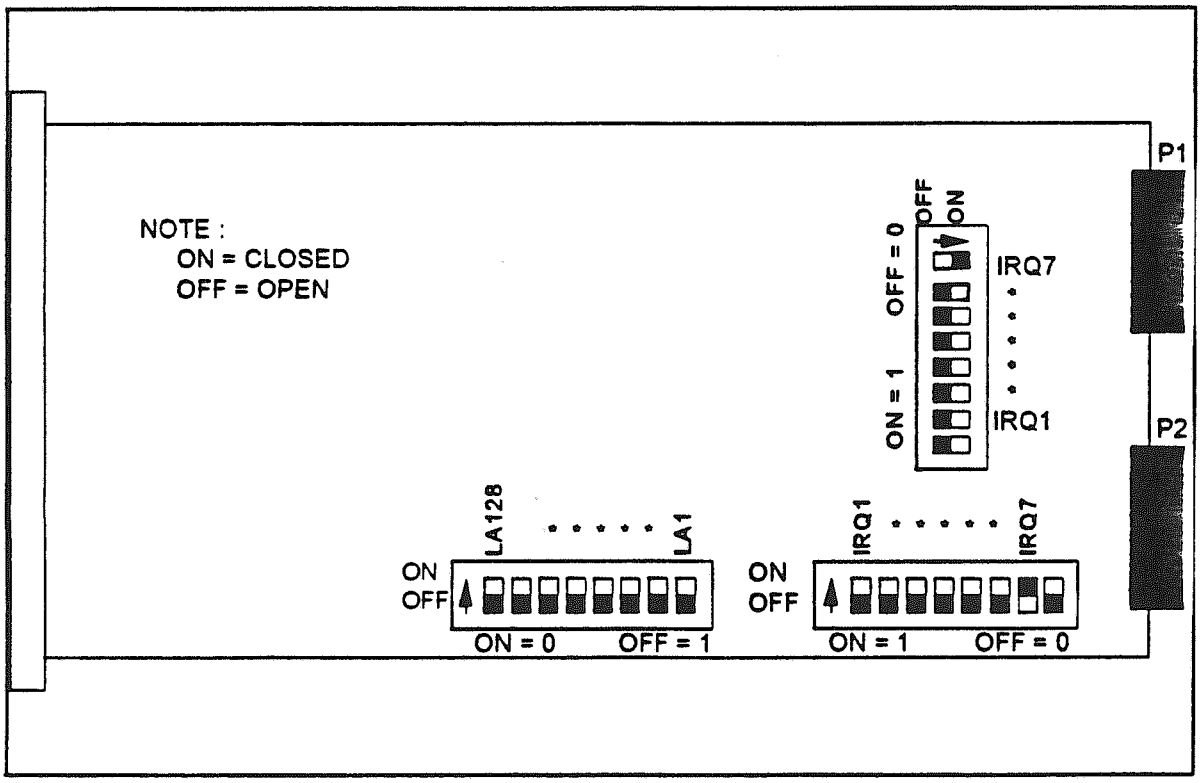


FIGURE 1 - V605 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to "1" (VXI defined).

Bits 13 through 6 are user-selectable via the address switches LA128-LA1.

Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V605 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 (page 3) for the switch locations and switch settings. Both banks of eight-position switches must be set to the same positions. As shown in Figure 1 (page 3) IRQ 7 is set in both banks.

Module Insertion

The V605 is a C-sized, single width VXIbus module. It requires 2600 milliamperes of +5 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE

To insure proper interrupt acknowledge cycles from the V605 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Daisy-chain jumpers must be installed in any empty slot between the V605 and the Slot 0 Controller.

FRONT PANEL INFORMATION

LEDs

ADD_REC — This LED is illuminated when the Operational Registers are being accessed.

INT ENA — This LED turns on when Enable INT Request Register (Operational Register offset $4A_{16}$) is read. Likewise, reading the Disable INT Request Register (Operational Register offset $4E_{16}$) will turn this LED off.

INT SRC — This LED turns on when any one of the six counter channels has set their interrupt status bit.

CONNECTORS

1-6, LATCH — These seven two-pin LEMO connectors will accept the output of a differential line-driver with the output characteristics like National's 8830. The inputs may also be configured for TTL inputs. Refer to Appendix for additional configuration options.A voltage signal of approximately 2.4 volts will turn on the optical-isolator. This voltage is considered a logical "1" for all the counter inputs, and the Latch input. The female contact facing the front, toward the left-hand side of the connector, is the more positive contact for the optical-isolator to turn-on. The counters are incremented on the transition from a logical "0" to a logical "1" of the input pulse. The optical-isolators provide an isolation voltage of 3000 volts DC. All input signals should have a minimum pulse width of 200 nanoseconds.

I — This single-pin LEMO connector is provided to inhibit the counters when a low-true signal level is applied.

KineticSystems' cable assemblies, Model 5857-Axyz through 5857-Dxyz, mate with the front-panel LEMO connectors.

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V605 implements those required for register-based devices. The V605 also contains a set of Operational Registers to monitor and control the functional aspects of the devices. Both register sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIbus Configuration Registers

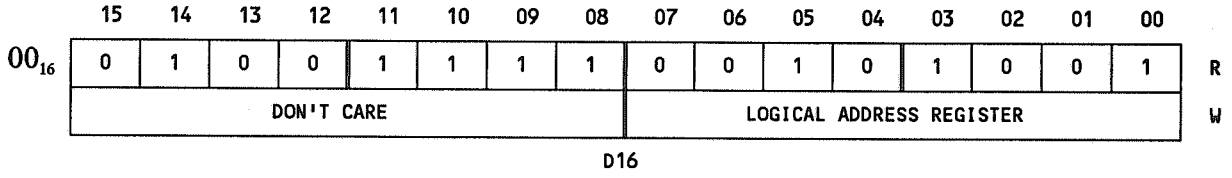
Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V605 are offset from the base address. **Note: The V605 only responds to these addresses if the Short Nonprivileged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle.** Table 1 (below) shows the applicable Configuration

Modifier Codes are set for the backplane bus cycle. Table 1 (below) shows the applicable Configuration Registers present in the V605, their offset from the base (Logical) address, and their Read/Write capabilities.

TABLE 1
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET (HEX)	W/R MODE	REGISTER NAME
00_{16}	W/R	ID/Logical Address Register
02_{16}	R	Device Type Register
04_{16}	W/R	Status/Control Register
06_{16}	W/R	Offset Register
08_{16}	R	Attribute Register
$1E_{16}$	R	Subclass Register

ID/Logical Address Register

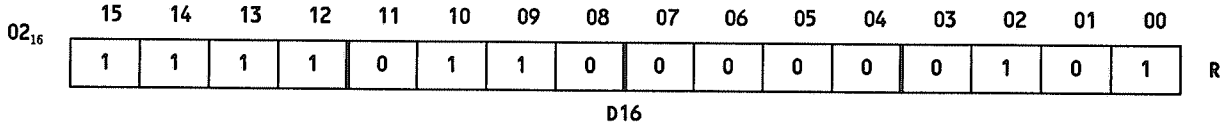


On READ transactions:

Bits(s)	Label	Meaning
15, 14	Device Class	This is a register-based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V605. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

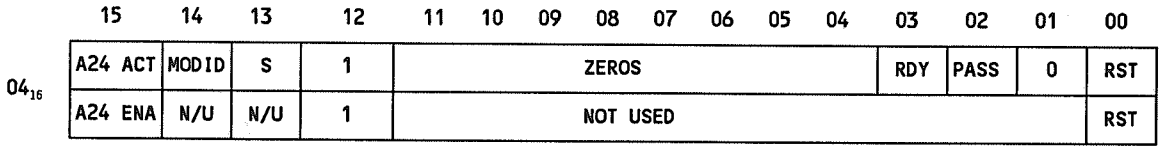
Device Type



On READ transactions:

Bit(s)	Label	Meaning
15 - 12	Required Memory	The V605 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model 605_{16}.

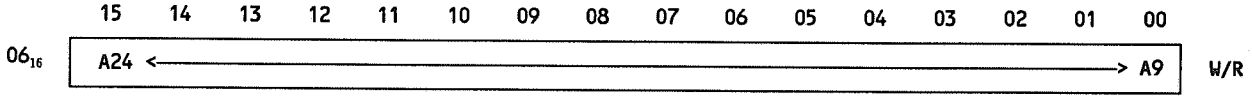
Status/Control Register



Bit	Mnemonics	Description
15	A24	Writing a "1" will enable A24 addressing and allow access to the Operational Registers. Reading a "1" indicates A24 is active. This bit is reset to a "0" on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected by the MODID line on VXIbus connector P2. A "0" will indicate that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V605. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1".
11-4	N/U	Not used. Read as "0"s.

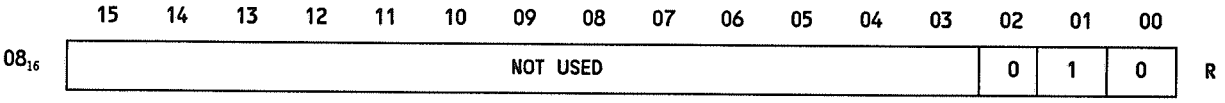
3	RDY	READY. The V605 is always ready. Read as a "1".
2	PASS	PASS. The V605 will always pass self tests. Read as a "1".
1	N/U	NOT USED. Read as a "0".
0	RST	RESET. This Read/Write bit controls the Soft Reset condition within the V605. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Register, except the Diagnostic and Interrupt Status registers, is inhibited. This bit can be reset by writing a "0", on power-up or the assertion of SYSRESET*.

Offset Register



This 16-bit read/write register defines the base address of this A24 Operational Registers. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Attribute Register



Bit(s)	Label	Meaning
15 - 03	Not Used	These bits are not used by the V605, and are read as "0"s.
02	Intr Control	Indicates Interrupt Control Capability
1	Intr Handler	Not an Interrupt Handler
00	Intr Status	Indicates Interrupt Status Capability

Subclass Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	R

Bit(s)	Label	Meaning
15	Extended Device	"1" indicates that this is a VXIbus defined Extended Device.
14-0	Register-Based	$7FFE_{16}$ indicates that this is an Extended Register Based Device.

OPERATIONAL REGISTERS

The Operational Registers are the mechanism used to access the functional registers of the V605. For compatibility with other KineticSystems' VXIbus modules in this series, these registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register. **Note: The V605 will only respond to these addresses if the Standard Nonprivileged Data Access (39 hex), Standard Nonprivileged Program Access (3A hex), Standard Supervisory Data Access (3D hex), or Standard Supervisory Program Access (3E hex) Address Modifier Codes are set for the bus cycle(s).**

Of the 256 bytes requested by the setting of the Device Type Register in the Configuration Register set, only 62 bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type Register.) Table 2 (below) shows the applicable Operational Registers present in the V605, their offset from the base A24 address, and their Read/Write capabilities.

TABLE 2
V605 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

A24 OFFSET	W/R MODE	REGISTER NAME
00_{16}	W/R	Diagnostic Register
02_{16}	W/R	Interrupt Status/ID Register
12_{16}	R	Channel #1 Low
14_{16}	R	Channel #1 High
16_{16}	R	Channel #2 Low
18_{16}	R	Channel #2 High
$1A_{16}$	R	Channel #3 Low

A24 OFFSET	W/R MODE	REGISTER NAME
$1C_{16}$	R	Channel #3 High
$1E_{16}$	R	Channel #4 Low
20_{16}	R	Channel #4 High
22_{16}	R	Channel #5 Low
24_{16}	R	Channel #5 High
26_{16}	R	Channel #6 Low
28_{16}	R	Channel #6 High
$2A_{16}$	R	Interrupt Status Register
$2E_{16}$	R	Increment all Channels
32_{16}	R	Enable Overflow INT Request
36_{16}	R	Disable Overflow INT Request
$3A_{16}$	R	Enable Ext. Latch INT Request
$3E_{16}$	R	Disable Ext. Latch INT Request
42_{16}	R	Clear Overflow INT Status #1
46_{16}	R	Clear Overflow INT Status #2
$4A_{16}$	R	Clear Overflow INT Status #3
$4E_{16}$	R	Clear Overflow INT Status #4
52_{16}	R	Clear Overflow INT Status #5
56_{16}	R	Clear Overflow INT Status #6
$5A_{16}$	R	Clear Ext. Latch INT Status

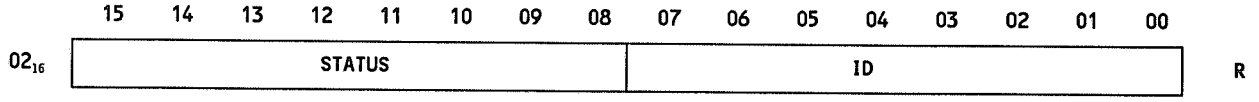
Diagnostic Register 00_{16}

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care								D	S	0	INT ENA	INT SRC	INH	0	0	R
00_{16}	Don't Care								0	0	0	INT ENA	0	INH	CLR	INIT	W

Bit	Mnemonic	Description
15-8	D/C	Don't Care.
7	Diagnostic	When this bit is set to a "1", the last register access to the Operational Registers (offsets 12_{16} through $5A_{16}$) is valid.
6	Status	When this bit is set to a "1", the last register access to the Operational Registers (offsets 12_{16} through $5A_{16}$) was accepted.
5	N/U	Not Used. Read as "0".
4	INT ENA	Interrupt Enable: Setting this bit to a "1" will enable interrupts.
3	INT SRC	Interrupt Source: When this bit is set to a "1", a V605 counter channel has overflowed.

2	INH	Inhibit: Setting this bit to a "1" will enable channel counting. This bit is always cleared on power-up or from a SYSRESET* and must be set to a "1" to enable the counting.
1	CLR	Setting this bit will clear the counters and the interrupt status bits.
0	INIT	Setting this bit to a "1" will only reset the Operational Registers (offsets 12_{16} through $5A_{16}$). The Configuration Registers and the Diagnostic Registers are unaffected.

Interrupt Status/ID Register



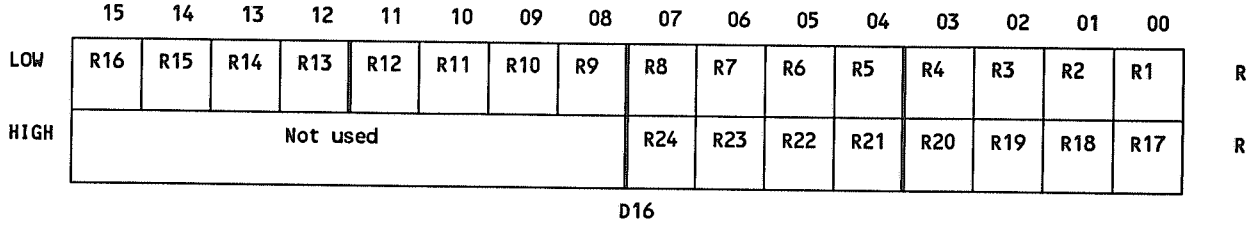
This is a Read-Only 16-bit Interrupt Status Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.

Bit	Mnemonic	Description
15-8	STATUS:	These eight bits will indicate Request True or Request False. Request True = FD_{16} Request False = FC_{16}
7-0	ID:	These eight bits represent the Logical Address of the V605 Configuration Registers.

Channel Counter Registers

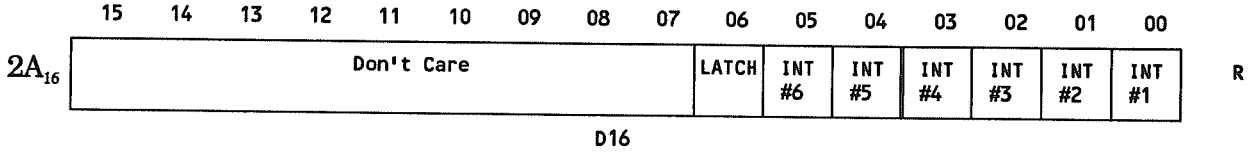
To read all 24-bits of the Channel Counter Register, a read to the LOW register must be executed before a read from the HIGH register can be made. The Low register will read the counter value for bits 1 through 16, while the High register will indicate the state of bits 17 through 24. The status bit in the Diagnostic Register will always equal a one when these registers (offsets 12_{16} through 28_{16}) are read. Refer to Table 2 for the register layout on the Channel Counter Registers.

Note: The INH bit must be written with a "1" in the Diagnostic Register to enable the counters.



Interrupt Status Register

This register is used to read out the interrupt status bits in the V605. These bits are set to indicate when a channel overflows its counting registers and are used to determine which counter has caused an interrupt, if the Interrupt request is enabled. A read from this register will always set the status bit in the Diagnostic Register to a "1". A register layout is shown below:



OPERATIONAL CONTROL REGISTERS

The V605 has 12 Operational Control Registers at offset $2E_{16}$ through $5A_{16}$. These registers are Read-Only and return a 16-bit data code. There are only two possible codes that can be returned. The first data code will return a value of zero and has the same meaning as the Status bit in the Diagnostic Register set to logical "0". The second data code will return a value of one and has the same meaning as the Status bit in the Diagnostic Register set to a logical "1". This data code will indicate the command was accepted or a test condition is true when equal to one. These 12 Operation Control Registers are described below:

Increment All Channels (Offset $2E_{16}$)

One increment pulse is generated for all channels for every read from this register. This register will always return a data value of one.

Enable Overflow INT Request (Offset 32_{16})
Disable Overflow INT Request (Offset 36_{16})

A read from either register will enable or disable Overflow INT Request. An Interrupt Request must be enabled if the V605 is going to set an interrupt. Both registers will return a data value of one.

Enable Ext. Latch INT Request (Offset $3A_{16}$)
Disable Ext. Latch INT Request (Offset $3E_{16}$)

A read from either register will enable or disable the External Latch INT Request. An Interrupt Request must be enabled if the V605 is going to set an interrupt. Both registers will return a data code of one.

Clear Overflow INT Status 1 through 6 (Offsets 42_{16} through 56_{16})

There are six registers so that each channel can be cleared individually. When a read operation is preformed to any one of these registers, the channel overflow interrupt status bit for that channel is cleared. These six registers will always return a data code of one.

Clear External Latch INT Status (Offset $5A_{16}$)

This register will clear the External Latch Interrupt status bit when a read operation is preformed. This register will always return a data code of one.

INHIBIT

Either the external inhibit signal or setting the INH bit in the Diagnostic Register to a logical "0" will prevent the counters from accepting clock pulses. Toggling of the Inhibit signal will not cause any false counts.

A low-level TTL signal on the external Inhibit line will prevent the counting process on the module. This output signal can be either a relay contact closure or an open-collector TTL device. A pull-up resistor is provided on the Inhibit input for these outputs. It is not necessary to terminate the external Inhibit signal when it is not used.

On crate power-up, the INH bit in the Diagnostic Register is cleared to a logical "0". This will inhibit any counting. One should set the INH bit to a logical "1" in the Diagnostic Register to allow counting.

INTERRUPTS

The V605 can generate an interrupt from one of six sources. Each channel can generate an interrupt when the counter overflows. The counter for a given channel overflows when the count exceeds 16,776,215 ($FFFFFF_{16}$).

The V605 must be setup properly in order to interrupt the VXIbus. First, the interrupt switches must select one of seven Interrupt Requests by switching the appropriate IRQ switches to the "ON" position. Next, enable interrupt in the following manner:

> Enable Interrupt Request by reading the ENA Overflow INT Request Register (offset 32_{16} in the Operational Register set).

Enable Interrupts to the VXIBUS by writing Bit 4 in the Diagnostic Register (offset 00_{16} in the Operational Register set) to a Logical "1".

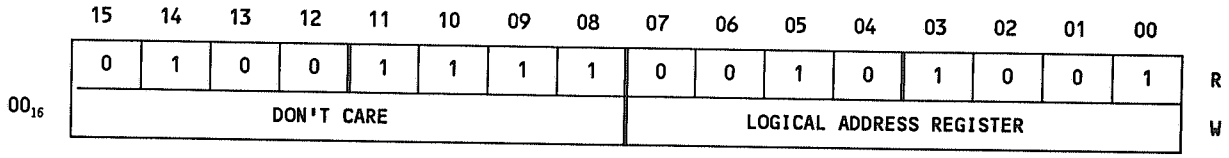
The V605 is now able to cause an interrupt on the VXIbus. Once the V605 sets an interrupt, an interrupt handler will read the Status/ID Register and reset the Enable Interrupt bit in the Diagnostic Register to a Logical "0". At this time, the interrupt request should be cleared which will also clear INT SRC in the Diagnostic Register to a Logical "0". To clear an Interrupt request, read the Interrupt Status Register to determine which interrupt status bit is causing the interrupt. Then clear the interrupt status bit with the appropriate clear function. Refer to Table 2, V605 Operational Registers, for a list of clear functions. Once INT SRC (Bit 3 in the Diagnostic Register) is set to a Logical "0", the Interrupt Enable (Bit 4 in the Diagnostic Register) can be set to a Logical "1". If INT SRC is a Logical "1" when INT ENA is set to a Logical "1", an interrupt will occur instantly.

APPENDIX A

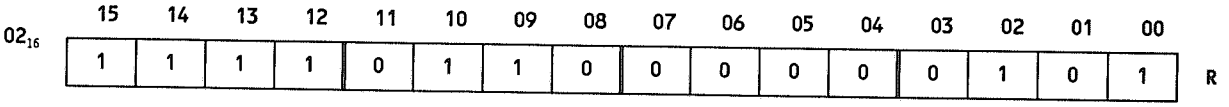
V605 REGISTER LAYOUT

CONFIGURATION REGISTERS

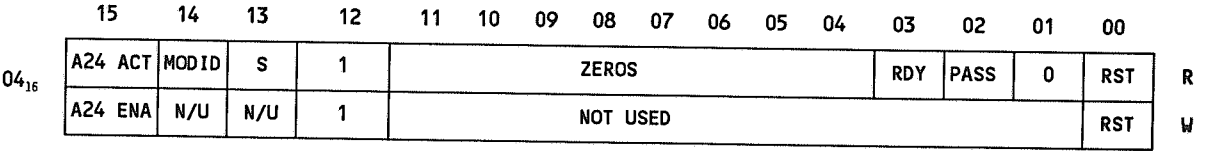
ID/Logical Address Register



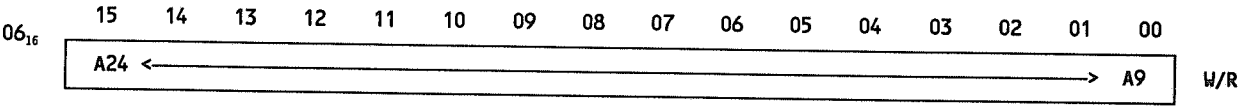
Device Type



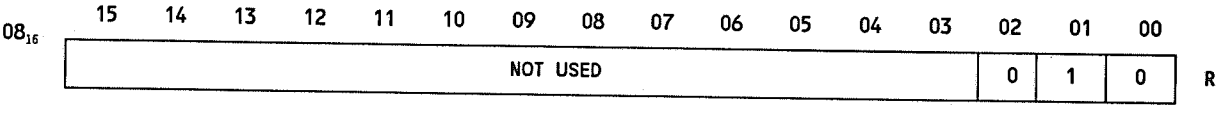
Status/Control Register



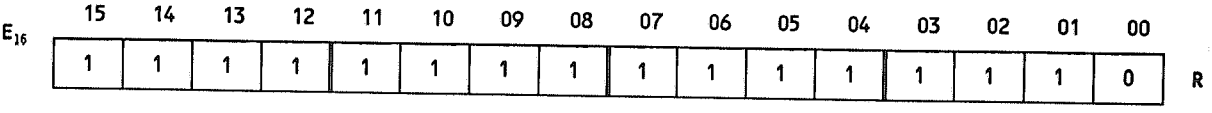
Offset Register



Attribute Register



Subclass Register



OPERATIONAL REGISTERS

00_{16}

Diagnostic Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care								D	S	0	INT ENA	INT SRC	0	0	0	R
	Don't Care								0	0	0	INT ENA	0	0	CLR	INIT	W

Interrupt Status/ID Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	STATUS								ID								R

Read Channel Counter Register

Channel	1	2	3	4	5	6
LOW	12_{16}	16_{16}	$1A_{16}$	$1E_{16}$	22_{16}	26_{16}
HIGH	14_{16}	18_{16}	$1C_{16}$	20_{16}	24_{16}	28_{16}

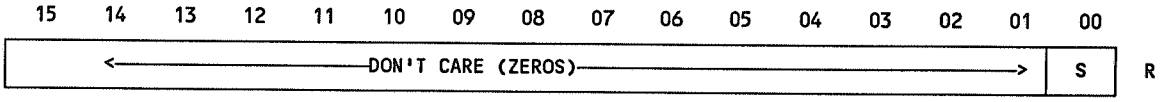
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
LOW	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
HIGH	Not used								R24	R23	R22	R21	R20	R19	R18	R17	R

Interrupt Status Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$2A_{16}$	Don't Care									LATCH	INT #6	INT #5	INT #4	INT #3	INT #2	INT #1	R

OPERATIONAL CONTROL REGISTERS

$2E_{16}$	**Increment All Channels**
32_{16}	**Enable Overflow INT Request**
36_{16}	**Disable Overflow INT Request**
$3A_{16}$	**Enable Ext. Latch INT Request**
$3E_{16}$	**Disable Ext. Latch INT Request**
42_{16}	**Clear Overflow INT Status Bit #1**
46_{16}	**Clear Overflow INT Status Bit #2**
$4A_{16}$	**Clear Overflow INT Status Bit #3**
$4E_{16}$	**Clear Overflow INT Status Bit #4**
52_{16}	**Clear Overflow INT Status Bit #5**
56_{16}	**Clear Overflow INT Status Bit #6**
$5A_{16}$	**Clear Ext. Latch INT Status**



S will be "1" if the control access was honored, "0" if not.

APPENDIX B

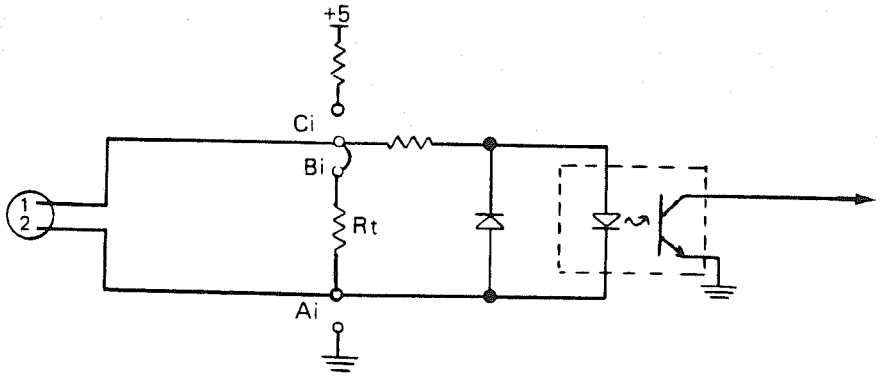
INPUT SELECTION

Each input can be strapped separately to accept either a TTL open-collector signal or a differential line-driver (8830 type) signal. If it is necessary to have the line-driver signal terminated, solder pad locations are provided for the user to insert a ¼ watt resistor. All input signals should have a minimum pulse width of 200 nanoseconds.

LINE-DRIVER INPUT

With Strap Bi loaded, the input will accept the output of a differential line-driver with the output characteristics like National's 8830. A voltage signal of approximately 2.4 volts will turn on the optical-isolator. This voltage is considered a logical "one" for all the counter inputs, and the Latch Input when the "NOR" strap is loaded. The female contact facing the front, toward the left-hand side of connector, should be the more positive contact for the optical-isolator to turn-on. The counters are incremented on the transition from a logical "zero" to a logical "one" of the input pulse. The optical-isolators provide an isolation voltage of 3000 volts DC in this configuration.

If the Latch Input is not used, strap the Latch Input to the driver and place the NOR/INV strap to the NOR position. The N•S2 must also be loaded if the Latch Input is not used.



Low = logical "one
for all counter inputs
and for latch input
when strapped "NOR"

Figure 2 - Straps loaded in Ai and Ci Open-Collector Input
Strap loaded in Bi Line Driver Input

TTL OPEN-COLLECTOR INPUT

A TTL Open-Collector output gate can drive each input two different ways. When both Ai and Ci are loaded, the open-collector output is connected to the positive input. A logical "zero" is the result of the output sinking at least 10 milliamps, and a logical "one" occurs when the output gate is turned off.

The output gate is connected to the negative input when strap Ai is removed and Ci is loaded. The logic convention for inputting a clock signal is the inverse of the previous paragraph.

Due to the addition of the pull-up resistor to the input circuit, the module's circuitry will not be isolated from the device supplying the signal to the V605.

If the Latch Input is not used, then strap the Latch Input to driver and place the NOR/INV strap to NOR position. The N•S2 must also be loaded if the Latch Input is not used.

INHIBIT

Either the INH bit in the Diagnostic Register (DRINH) or an external inhibit signal can prevent the counters from accepting clock pulses. Toggling of the Inhibit lines will not cause any false counts. The DRINH line may be enabled of disabled by a jumper.

A low-level TTL signal on the external Inhibit line will prevent the counting process on the module. This output signal can be either a relay contact closure or an open-collector TTL device. A pull-up resistor is provided on the Inhibit Input for these outputs. It is not necessary to terminate the external Inhibit signal when it is not used.

LATCH AND CLEAR MODE

After every eternal Latch signal is received, a clear pulse is generated. This clear pulse can be gated to each channel by loading the appropriate LCi strap (i=0 to 5). So, after the latch signal has stored the counters value into the output register, the clear pulse is sent to the selected channels to clear the counter and LAM status bit. This latch and clear mode works only for the External Latch signal.

STRAPS

LCO-LC5	When loaded, this strap will clear the appropriate channel after the Latch Signal has clocked the counter's value into the shift register. One strap is provided per channel.
A, B	With Strap A loaded, that channel will set the LAM status after the counters overflow the 24th bit. Loading the strap into location B, the LAM status bit is set on 16-bit overflow. Each channel has its own strap. These straps are located in a column starting by chip AL. Each channe will continue to count after it has overflowed.
Ai, Bi, Ci*	Selects if either a Line Driver or TTL open-collector signal will be accepted by the input. Load Ai and Ci for TTL open-collector input. Load Bi for Line Driver input.
AL, BL, CL	Latch Input
A0, B0, C0	Channel 0 Input
A1, B1, C1	Channel 1 Input
A2, B2, C2	Channel 2 Input
A3, B3, C3	Channe 3 Input
A4, B4, C4	Channel 4 Input
A5, B5, C5	Channel 5 Input
INH	Inhibit Enabled to Inhibit counting via Diagnostic Register Inhibit
$\overline{\text{INH}}$	Inhibit Disabled - Diagnostic Register INHIBIT has no effect.
.S2*	With this strap loaded, the counters output register will be updated every time the V605 is addressed. The latch strap should be set to "NOR".
NOR*	This strap is loaded when a high true latch signal is used.
INV*	For use with a low true latch signal.
*NOTE: Refer to TTL open-collector or Driver Input section for proper operation.	

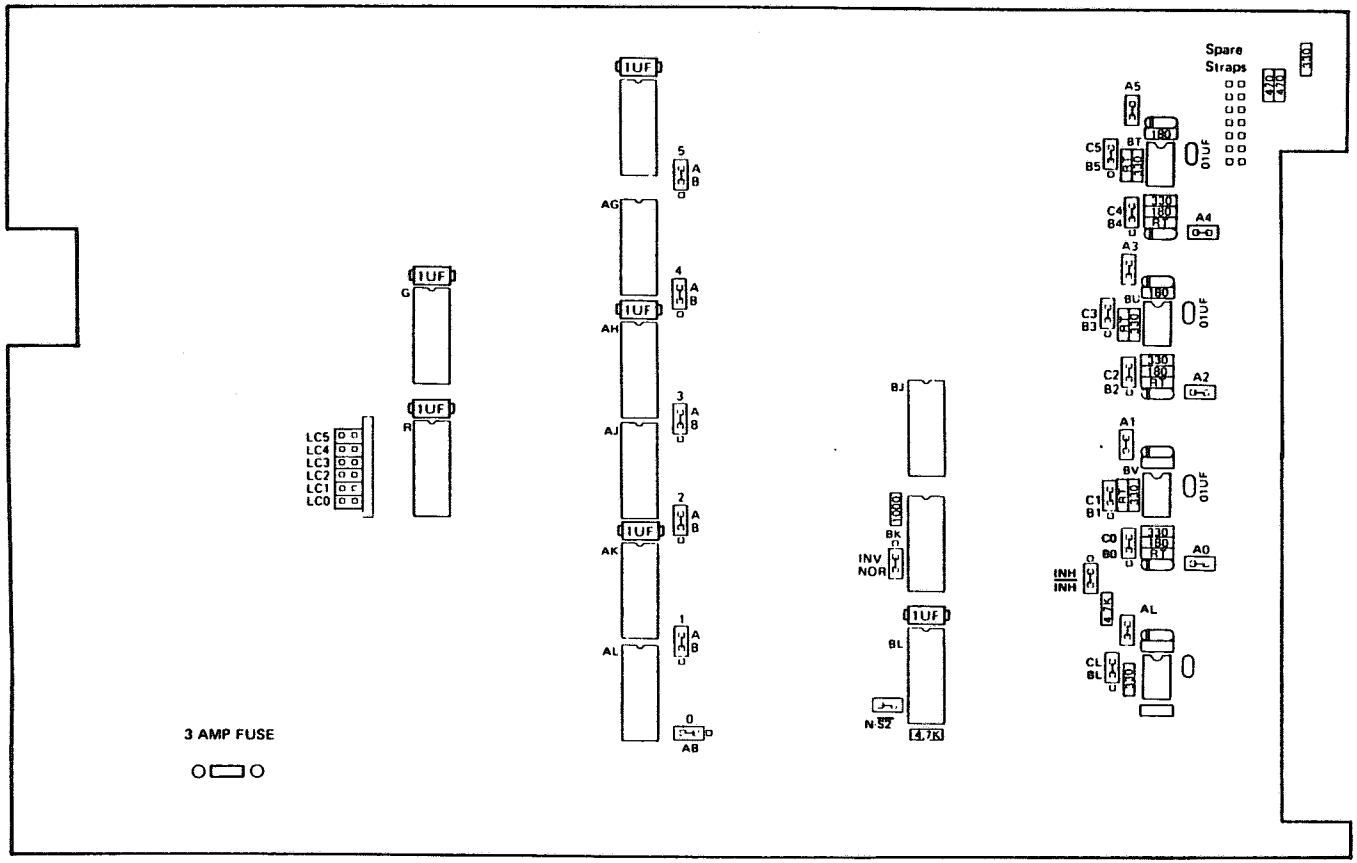


FIGURE 3 - V605 Strap Locations