Model V610-LA11/LB11

6-Channel, 50 MHz Counter

INSTRUCTION MANUAL

March, 1998

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FIGURES

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Warranty
NPD:rem(WP)

6-channel, 50 MHz Counter

Counts from dc to 50 MHz with TTL or NIM-level signals

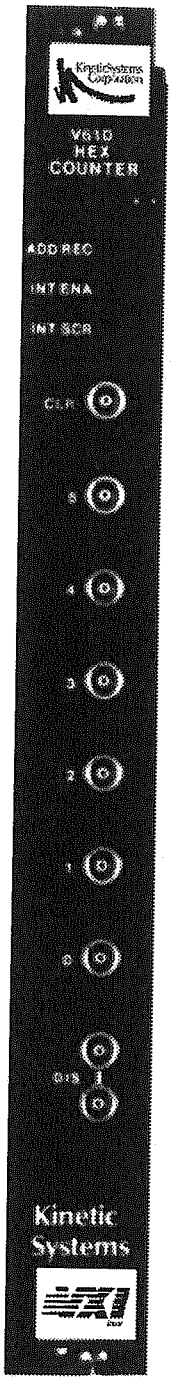
V610

Features

- **Six counters**
- **Maximum count of 24 bits (16,777,215) on each channel**
- **TTL or NIM input**
- **Interrupt on overflow**
- **dc to 50 MHz count rate**

Typical Applications

- **High energy physics experiments**
- **High-frequency counting applications**

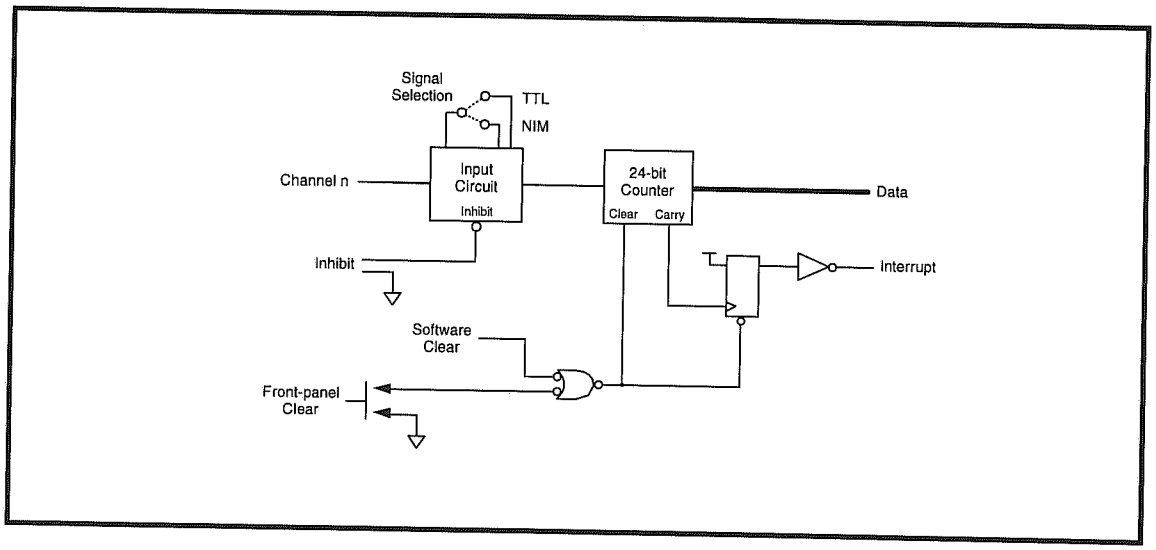


General Description *(Product specifications and descriptions subject to change without notice.)*

The V610 is a single-width, C-size, register-based, VXIbus module that contains six independent 24-bit counters. The maximum clock rate of the input signals is 50 MHz, and options are available for accepting either NIM or TTL level input signals. (The nominal NIM signal input is -16 mA into 50 W for a logical "one", and 0 mA for a logical "zero".) An external Inhibit signal (of the same signal type as the inputs) can be used to gate off all counters. Each counter has an overflow bit which is set on a carry from bit 24, and generates an interrupt, if enabled. Counters continue to increment after the overflow condition has occurred. The pattern of overflow bits can be read via software. The counters can be individually cleared by software commands, or as a group by a software command or front-panel-mounted, manual, push-button switch. All inputs are protected for a ±50 V transient or ±4 V dc.

The V610 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.

A Typical Counter Channel



V610 *(continued)*

Item	Specification
Number of Channels	6
Input Signal Levels	
TTL option	
Logic "0"	0.0 V to 0.8 V
Logic "1"	2.4 V to 5.0 V
NIM option	
Logic "0"	0 mA into 50 Ω
Logic "1"	-16 mA into 50 Ω
Input Protection	±4 V dc, ±50 V transient
Maximum Clock Rate (per channel)	50 MHz
Maximum Count Value	16,777,215 (24 bits)
Input Connector Type	Single-pin LEMO receptacle, shell size 00
Mating Connectors	KineticSystems Model 5910-Z1A
Power Requirements	
+5 V	2.4 A, typical
-5.2 V	330 mA, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-sized VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V610-LA11 6-channel 50 MHz Counter, TTL inputs
Model V610-LB11 6-channel 50 MHz Counter, NIM inputs

Related Products

Model 5857-Axyz Cable—1-contact LEMO to Unterminated
Model 5857-Bxyz Cable—1-contact LEMO to 1-contact LEMO
Model 5857-Hxyz Cable—1-contact LEMO to BNC shielded
Model 5910-Z1A Connector—1-contact LEMO

UNPACKING AND INSTALLATION

The Model V610 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V610 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V610 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. (Refer to FIGURE 1 below.)

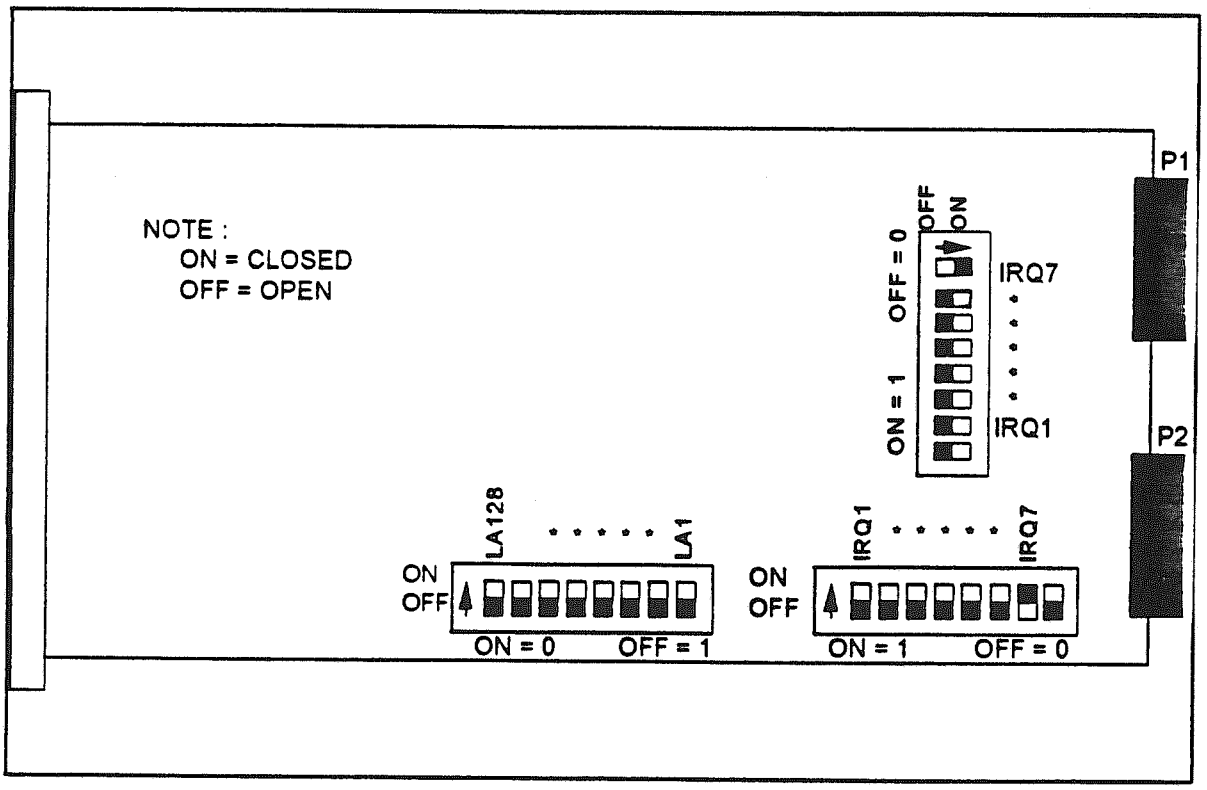


FIGURE 1 - V610 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

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The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to "1" (VXI defined).

Bits 13 through 6 are user-selectable via the address switches LA128-LA1.

Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V610 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 for the switch locations and switch settings. Both banks of eight-position switches must be set to the same position. As shown in Figure 1, IRQ 7 is set to the same position in both banks.

Module Insertion

The V610 is a C-sized, single width VXIbus module. It requires 2400 milliamperes of +5 volt power, 330 milliamperes of -5 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame.

CAUTION:	TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING:	REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE

To insure proper interrupt acknowledge cycles from the V610 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V610 and the Slot 0 Controller.

FRONT PANEL INFORMATION

LEDs

ADD_REC — This LED turns on when the Operational Registers are being accessed.

INT ENA — This LED turns on when the Enable INT Request Register ($4A_{16}$) is read. Likewise, reading Disable INT Request Register ($4E_{16}$) will turn this LED off.

INT SRC — This LED turns on when any one of the six channels has set its interrupt status bit.

CONNECTORS

1-6 — These six single-pin LEMO connectors are the inputs to channels 1 through 6. These input are low-true TTL signals and represent one Schottky TTL load.

I — Two single-pin LEMO connectors are provided to inhibit the counting when a low-true signal is applied. These two connectors are bridged to provide for "Daisy Chaining" with other V610 modules.

Pushbutton

CLEAR — This Pushbutton will clear all the counters and the Interrupt Status Register.

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V610 implements those required for register-based devices. The V610 also contains a set of Operational Registers to monitor and control the functional aspects of the devices. Both registers sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIbus Configuration Registers

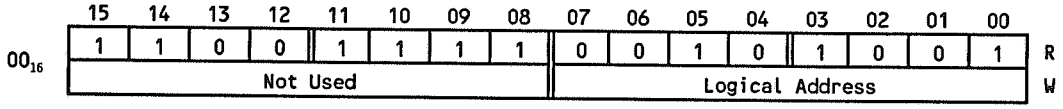
Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V610 are offset from the base address. **Note: the V610 only responds to these addresses if the Short Nonprivileged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle.** Table 1 shows the applicable Configuration Registers present in the V610, their offset from the base (Logical) address, and their Read/Write capabilities.

Table 1 - Configuration Registers - Short I/O Address Space

OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Read/Write	Status/Control Register
06_{16}	Read/Write	Offset Register
08_{16}	Read Only	Attribute Register
$1E_{16}$	Read Only	Subclass Register

ID/Logical Address Register

The format and bit assignments for the ID/Logical Address Register are as follows:



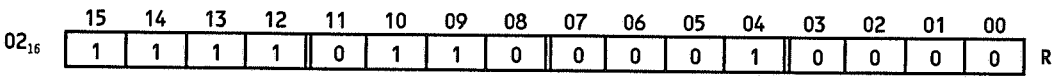
On READ transactions:

Bit(s)	Mnemonic	Description
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V610. In Dynamically configured systems (i.e., the Logical Address switches are set to a value of 255), bits seven through zero are written with the new Logical Address value.

Device Type Register

The format and bit assignments for the Device Type Register are as follows:



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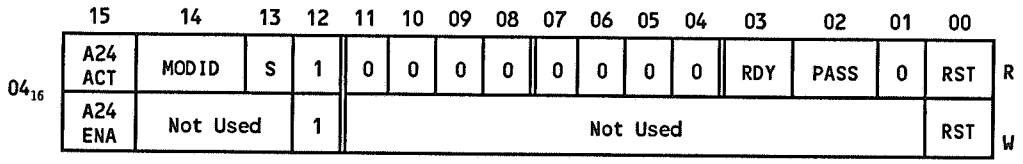
Bit(s)	Mnemonic	Description
15 - 12	Required Memory	The V610 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model V610 (610_{16}).

Status/Control Register

The format and bit assignments for the Status/Control Register are as follows:

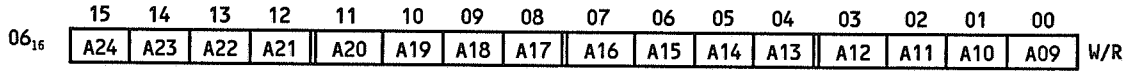


Bit(s)	Mnemonic	Meaning
15	A24 Enable	This bit is written with a "1" to enable A24 addressing and reset (to "0") to disable A24 addressing. **This bit <u>must</u> be set to "1" to allow access to the module's Operational Registers.** Reads of this bit indicate its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is <u>not</u> selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V610. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems' VXIbus modules. It should always be written with a "1."
11 - 04	Not Used	When read, will return all "0"s. These bits are ignored when written.
03	Ready	Along with Bit 02 (Passed), this Read-Only bit will appear as a "1" to indicate its readiness to accept operational commands.
02	Passed	See the Ready bit description.

01	Not Used	Read as "0" and ignore on write transactions.
00	Reset	This Read/Write bit controls the Soft Reset condition within the V610. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Registers (see below) is inhibited. This bit is reset by writing a "0", on power-up or the assertion of SYSRESET*.

Offset Register

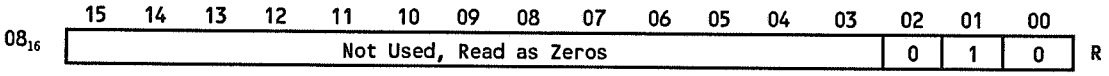
The format and bit assignments for the Offset Register are as follows:



This Read/Write register defines the base address of the V610's Operational Registers. These 16 bits contain the 16 most significant bits of the module's A24 space register addresses. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Interrupt Attribute Register

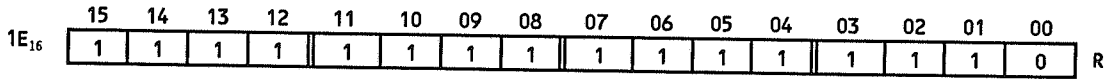
The format and bit assignments for the Interrupt Attribute Register are as follows:



Bit(s)	Mnemonic	Description
15 - 03	Not Used	These bits are not used by the V610, and are read as zeros.
02	Intr Control	Indicates Interrupt Control capability.
01	Intr Handler	No Interrupt Handler capabilities.
00	Intr Status	Indicates Interrupt Status capability.

Subclass Register

The format and bit assignments for the Subclass Register are as follows:



Bit(s)	Mnemonic	Description
15	Extended Device	"1" indicates that this is a VXIbus defined Extended Device.
14-00	Register-Based	$7FFE_{16}$ indicates that this is an Extended register-based Device.

Operational Registers

The Operational Registers are the channels through which the input count values of the V610 are read. For compatibility with other KineticSystems' VXIbus modules in this series, these registers are positioned in VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register (see page 7). **Note: The V610 will only respond to these addresses if the Standard Nonprivileged Data Access (39_{16}), Standard Nonprivileged Program Access ($3A_{16}$), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for the bus cycle(s).**

Of the 256 bytes requested by the setting of the Device Type register in the Configuration Register set, only 130 bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type register.) Table 2 shows the applicable Operational Registers present in the V610, their offset from the base A24 address, and their Read/Write capabilities.

Table 2 - V610 Operational Registers - Standard Address Space

A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	READ/WRITE	Diagnostic Register
02_{16}	READ/WRITE	Interrupt Status/ID Register
12_{16}	READ	Channel #1 Low
14_{16}	READ	Channel #1 High
16_{16}	READ	Channel #2 Low
18_{16}	READ	Channel #2 High
$1A_{16}$	READ	Channel #3 Low

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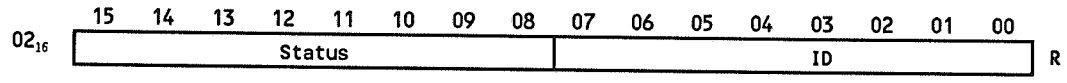
A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
$1C_{16}$	READ	Channel #3 High
$1E_{16}$	READ	Channel #4 Low
20_{16}	READ	Channel #4 High
22_{16}	READ	Channel #5 Low
24_{16}	READ	Channel #5 High
26_{16}	READ	Channel #6 Low
28_{16}	READ	Channel #6 High
$2A_{16}$	READ	Read & Clear Channel #1 Low/INT #1
$2C_{16}$	READ	Read & Clear Channel #1 High/INT #1
$2E_{16}$	READ	Read & Clear Channel #2 Low/INT #2
30_{16}	READ	Read & Clear Channel #2 High/INT #2
32_{16}	READ	Read & Clear Channel #3 Low/INT #3
34_{16}	READ	Read & Clear Channel #3 High/INT #3
36_{16}	READ	Read & Clear Channel #4 Low/INT #4
38_{16}	READ	Read & Clear Channel #4 High/INT #4
$3A_{16}$	READ	Read & Clear Channel #5 Low/INT #5
$3C_{16}$	READ	Read & Clear Channel #5 High/INT #5
$3E_{16}$	READ	Read & Clear Channel #6 Low/INT #6
40_{16}	READ	Read & Clear Channel #6 High/INT #6
42_{16}	READ	Interrupt Status Register
46_{16}	READ	Increment all Channels
$4A_{16}$	READ	Enable INT Request
$4E_{16}$	READ	Disable INT Request
56_{16}	READ	Clear Channel / INT Status #1
$5A_{16}$	READ	Clear Channel / INT Status #2
$5E_{16}$	READ	Clear Channel / INT Status #3
62_{16}	READ	Clear Channel / INT Status #4
66_{16}	READ	Clear Channel / INT Status #5
$6A_{16}$	READ	Clear Channel / INT Status #6
$6E_{16}$	READ	Clear INT Status #1
72_{16}	READ	Clear INT Status #2
76_{16}	READ	Clear INT Status #3
$7A_{16}$	READ	Clear INT Status #4
$7E_{16}$	READ	Clear INT Status #5
82_{16}	READ	Clear INT Status #6

Diagnostic Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care								D	S	0	INT ENA	INT SRC	INH	0	0	R
00_{16}	Don't Care								0	0	0	INT ENA	0	INH	CLR	INIT	W

Bit(s)	Mnemonic	Description
15 - 08	Not Used	On Read transactions, these bits return an all "0" pattern. On Write transactions, these bits are ignored by the module.
07	Diagnostic	When this bit is set to a "1", the last register access to the Operational Registers (offsets 12_{16} through 82_{16}) was valid.
06	Status	When this bit is set to a "1", the last register access to the Operational Registers (offsets 12_{16} through 82_{16}) was accepted.
05	Not Used	Read as "0"s, ignored on write cycles.
04	INT ENA	Interrupt Enable: setting this bit to a "1" will enable interrupts.
03	INT SRC	Interrupt Source: When this bit is set to a "1", a V610 counter channel has overflowed.
02	INH	Inhibit: setting this bit to a "1" will enable channel counting. This bit is always cleared on power-up or from a SYSRESET*, and must be set to a "1" to enable the counters.
01	CLR	Setting this bit will clear the counters and the interrupt status bits.
00	INIT	Setting this bit to a "1" will only reset the Operational Registers (offsets 12_{16} through 82_{16}). The Configuration Registers and the Diagnostic Register are unaffected.

Interrupt Status/ID Register



This is a read only 16-bit Interrupt Vector Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.

Bit(s)	Mnemonic	Description
15 - 08	STATUS	These eight bits will indicate Request True or Request False. Request True = FD_{16} Request False = FC_{16}
07 - 00	ID	These eight bits represent the Logical Address as set in the V610 Configuration Registers.

Channel Counter Register

To read all 24 bits of a Channel Counter register, a read to the LOW register must executed first before a read from the HIGH register can be read. The Low register will read the input state for bits one through 16, while the High register will indicate the state for bits 17 through 24. The status bit in the Diagnostic Register will always be equal a one when these registers (12_{16} through 28_{16}) are read.

Note: The INH bit must be written with a "1" in the Diagnostic Register to enable the counting registers.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
LOW	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
HIGH	Not Used								R24	R23	R22	R21	R20	R19	R18	R17	R

A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
12_{16}	READ	Channel #1 Low
14_{16}	READ	Channel #1 High
16_{16}	READ	Channel #2 Low
18_{16}	READ	Channel #2 High
$1A_{16}$	READ	Channel #3 Low
$1C_{16}$	READ	Channel #3 High
$1E_{16}$	READ	Channel #4 Low
20_{16}	READ	Channel #4 High
22_{16}	READ	Channel #5 Low
24_{16}	READ	Channel #5 High
26_{16}	READ	Channel #6 Low
28_{16}	READ	Channel #6 High

Read & Clear Channel Counter Registers

A read from these registers will read all 24 bits from a counter register and then clear the counter register to zero. This operation will also clear the Interrupt status bit associated with a given channel. To read all 24 bits of the channel counter register, a read to the LOW register must be executed before a read to the HIGH register can be made. The Low register will contain the counter state for bits 1 through 16, while the High register will indicate the state for bits 17 through 24. The status bit in the Diagnostic Register will always be equal to "1" when these registers ($2A_{16}$ through 40_{16}) are read.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
LOW	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
HIGH	Not Used.								R24	R23	R22	R21	R20	R19	R18	R17	R

A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
$2A_{16}$	READ	Read & Clear Channel #1 Low/INT #1
$2C_{16}$	READ	Read & Clear Channel #1 High/INT #1
$2E_{16}$	READ	Read & Clear Channel #2 Low/INT #2
30_{16}	READ	Read & Clear Channel #2 High/INT #2
32_{16}	READ	Read & Clear Channel #3 Low/INT #3
34_{16}	READ	Read & Clear Channel #3 High/INT #3
36_{16}	READ	Read & Clear Channel #4 Low/INT #4
38_{16}	READ	Read & Clear Channel #4 High/INT #4
$3A_{16}$	READ	Read & Clear Channel #5 Low/INT #5
$3C_{16}$	READ	Read & Clear Channel #5 High/INT #5
$3E_{16}$	READ	Read & Clear Channel #6 Low/INT #6
40_{16}	READ	Read & Clear Channel #6 High/INT #6

Interrupt Status Register

This register is used to read out the Interrupt Status bits in the V610. These bits are set to indicate that a channel has overflowed its counting registers, and are read to determine which counter has caused an interrupt (if an Interrupt Request is enabled). A read from this register will always set the status bit in the Diagnostic Register to a "1". A register layout is shown below:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
42_{16}	Don't Care										INT #6	INT #5	INT #4	INT #3	INT #2	INT #1	R

Operational Control Registers

The V610 has nine Operational Control Registers at offsets $4A_{16}$ through $6E_{16}$. These registers are Read-Only and return a 16-bit data code. There are only two possible codes that can be returned. The first data code will return a value of "0". The second data code will return a value of "1". This code has the same meaning as the Status bit in the Diagnostic Register. When equal to "1", this data code indicates that the command was accepted or that a test condition is true. These sixteen Operational Control Registers are described below:

Increment All Channels (offset 46_{16})

For every read from this register, the count in each channel is incremented by one. This register will always return a data code of "1".

Enable INT Request (offset $4A_{16}$)
Disable INT Request (offset $4E_{16}$)

A read from either register will enable or disable INT Request. The Interrupt Request must be enabled if the V610 is going to set an interrupt. Both registers will return a data code of "1".

Clear Channel/INT Status

There are six registers (56_{16} through $6A_{16}$), one to clear each channel. When a read operation is performed on any one of these registers, the associated channel count register and interrupt status bit are cleared. These six registers will always return a data code of "1".

Clear INT Status

There are six registers ($6E_{16}$ through 82_{16}), one to clear each channel. When a read operation is performed to any one of these registers, the associated channel interrupt status bit is cleared. These six registers will always return a data code of "1".

INTERRUPTS

The V610 can generate interrupts from any one of six sources. Each channel can generate an interrupt when the counter overflows. The counter for a given channel overflows when the count exceeds 16,776,960 ($FFFFFF_{16}$).

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The V610 must be set up properly in order to interrupt the VXIbus. First, the interrupt switches must select one of seven Interrupt Requests by switching the appropriate IRQ switches to the "ON" position. Refer to the Interrupt Request Switch Selection for further information. Next, enable interrupt in the following manner:

Enable Interrupt Request by reading the ENA INT Request register for the desired channel(s).

Enable Interrupts to the VXIBUS by writing Bit 4 in the Diagnostic Register with a Logical "1".

The V610 is now capable of causing an interrupt on the VXIbus. Once the V610 sets an interrupt, an interrupt handler will read the Status/ID Register and reset the Enable Interrupt bit in the Diagnostic Register to a logical "0". At this time, the interrupt request should be cleared. This will also clear INT SRC in the Diagnostic Register to a Logical "0". To clear an Interrupt request, read the Interrupt Status Register to determine which interrupt status bit is causing the interrupt. Then clear the interrupt status bit with the appropriate clear function. Refer to Table 2, V610 Operational Registers, for a list of clear functions. Once INT SRC (Bit 3 in the Diagnostic Register) is set to a logical "0", the INT ENA (Bit 4 in the Diagnostic Register) can be set to a logical "1". If INT SRC is set to a logical "1" when INT ENA is set to a logical "1", an interrupt will occur instantly.

APPENDIX

V610 REGISTER LAYOUTS

Configuration Registers - Short I/O Address Space

OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Read/Write	Status/Control Register
06_{16}	Read/Write	Offset Register
08_{16}	Read Only	Attribute Register
$1E_{16}$	Read Only	Subclass Register

Configuration Register Formats

ID/LOGICAL ADDRESS REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	1	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1	R
	Not Used								Logical Address								W

DEVICE TYPE REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	1	1	1	1	0	1	1	0	0	0	0	1	0	0	0	0	R

STATUS/CONTROL REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
04_{16}	A24 ACT	MODID	S	1	0	0	0	0	0	0	0	0	RDY	PASS	0	RST	R
	A24 ENA	Not Used		1	Not Used											RST	W

OFFSET REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
06_{16}	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	W/R

INTERRUPT ATTRIBUTE REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
08_{16}	Not Used, Read as Zeros													0	1	0	R

SUBCLASS REGISTER

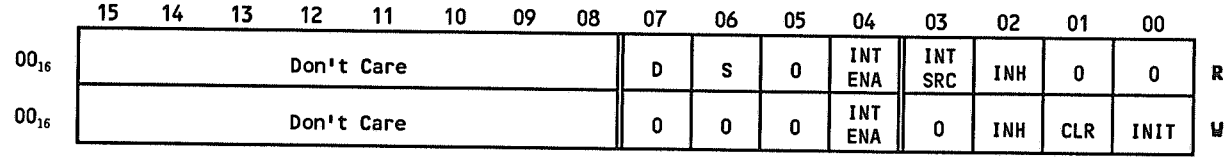
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	R

Operational Registers - Standard Address Space

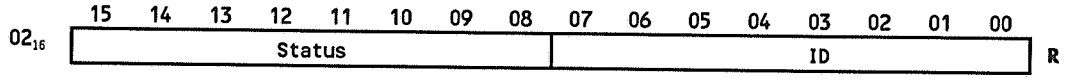
A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	READ/WRITE	Diagnostic Register
02_{16}	READ/WRITE	Interrupt Status/ID Register
12_{16}	READ	Channel #1 Low
14_{16}	READ	Channel #1 High
16_{16}	READ	Channel #2 Low
18_{16}	READ	Channel #2 High
$1A_{16}$	READ	Channel #3 Low
$1C_{16}$	READ	Channel #3 High
$1E_{16}$	READ	Channel #4 Low
20_{16}	READ	Channel #4 High
22_{16}	READ	Channel #5 Low
24_{16}	READ	Channel #5 High
26_{16}	READ	Channel #6 Low
28_{16}	READ	Channel #6 High
$2A_{16}$	READ	Read & Clear Channel Low/INT #1
$2C_{16}$	READ	Read Channel #1 High
$2E_{16}$	READ	Read & Clear Channel Low/INT #2
30_{16}	READ	Read Channel #2 High
32_{16}	READ	Read & Clear Channel Low/INT #3
34_{16}	READ	Read Channel #3 High
36_{16}	READ	Read & Clear Channel Low/INT #4
38_{16}	READ	Read Channel #4 High
$3A_{16}$	READ	Read & Clear Channel Low/INT #5
$3C_{16}$	READ	Read Channel #5 High
$3E_{16}$	READ	Read & Clear Channel Low/INT #6
40_{16}	READ	Read Channel #6 High
42_{16}	READ	Interrupt Status Register
46_{16}	READ	Increment all Channels
$4A_{16}$	READ	Enable INT Request
$4E_{16}$	READ	Disable INT Request
56_{16}	READ	Clear Channel / INT Status #1
$5A_{16}$	READ	Clear Channel / INT Status #2
$5E_{16}$	READ	Clear Channel / INT Status #3
62_{16}	READ	Clear Channel / INT Status #4
66_{16}	READ	Clear Channel / INT Status #5
$6A_{16}$	READ	Clear Channel / INT Status #6
$6E_{16}$	READ	Clear INT Status #1
72_{16}	READ	Clear INT Status #2
76_{16}	READ	Clear INT Status #3
$7A_{16}$	READ	Clear INT Status #4
$7E_{16}$	READ	Clear INT Status #5
82_{16}	READ	Clear INT Status #6

Operational Register Formats

DIAGNOSTIC REGISTER



INTERRUPT STATUS/ID REGISTER

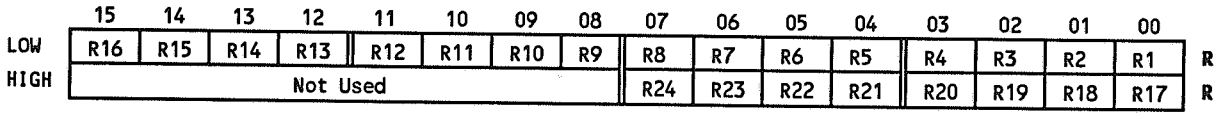


READ CHAN COUNTER REGISTER

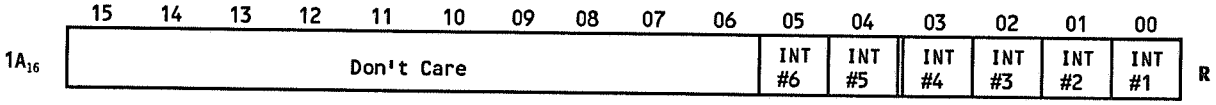
Channel	1	2	3	4	5	6
LOW	12_{16}	16_{16}	$1A_{16}$	$1E_{16}$	22_{16}	26_{16}
HIGH	14_{16}	18_{16}	$1C_{16}$	20_{16}	24_{16}	28_{16}

READ & CLEAR CHAN COUNTER REGISTER

LOW $2A_{16}$, $2E_{16}$, 32_{16}, 36_{16}, $3A_{16}$, $3E_{16}$
HIGH $2C_{16}$, 30_{16}, 34_{16}, 38_{16}, $3C_{16}$, 40_{16}



INTERRUPT STATUS REGISTER



OPERATIONAL CONTROL REGISTERS

46_{16}	Increment All Counters
$4A_{16}$	Enable INT Request
$4E_{16}$	Disable INT Request
52_{16}	Clear Channel/INT Status #1
56_{16}	Clear Channel/INT Status #2
$5A_{16}$	Clear Channel/INT Status #3
$5E_{16}$	Clear Channel/INT Status #4
62_{16}	Clear Channel/INT Status #5
66_{16}	Clear Channel/INT Status #6
$6A_{16}$	Clear INT Status Bit #1
$6E_{16}$	Clear INT Status Bit #2
72_{16}	Clear INT Status Bit #3
76_{16}	Clear INT Status Bit #4
$7A_{16}$	Clear INT Status Bit #5
$7E_{16}$	Clear INT Status Bit #6