Model V620-LA11

4-Channel Up/Down Presettable Counter

INSTRUCTION MANUAL

March, 1998

Special Option

Model V620-S001

4-channel, Up/Down Presettable
Counter

September, 1996

*****Special Option*****

Model V620-S001

The Model V620-S001 is the same as the V620-LA11 except it has been modified to take interrupt to VXI Trigger line and be enabled by VXI Trigger.

September 17, 1996

CONTENTS

4-channel, Up/Down Presettable Counter

Counts up or down from dc to 20 MHz with TTL-level signals

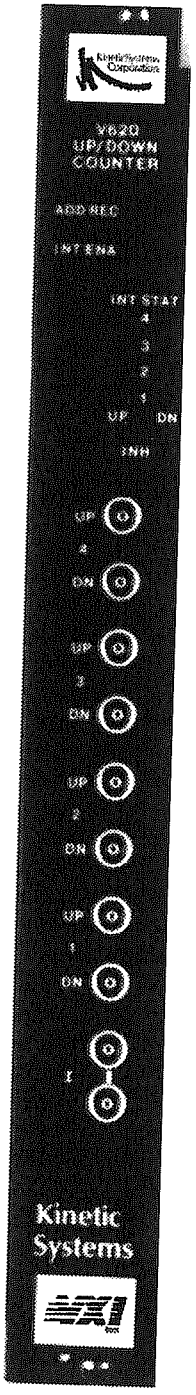
V620

Features

- **TTL-level inputs**
- **Counting rates from dc to 20 MHz**
- **Separate up/down inputs**
- **Capacity of 65,535 counts per channel**
- **Overflow and underflow interrupt source bits for each channel**
- **Separate clear command for each channel**

Typical Applications

- **Test cells**
- **Nuclear accelerator control and monitoring**
- **General-purpose counting**



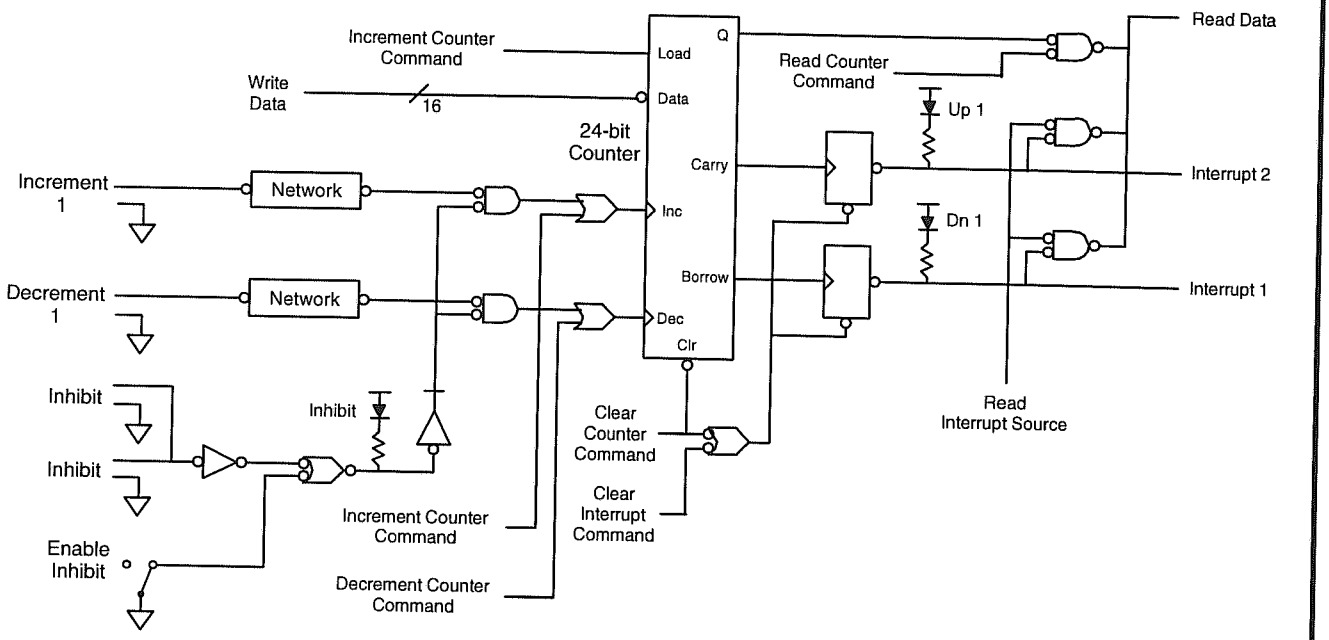
General Description *(Product specifications and descriptions subject to change without notice.)*

The V620 is a single-width, C-size, register-based, VXIbus module that contains four independent, presettable, 16-bit up-down counters. These counters accept TTL signals at rates ranging from dc to 20 MHz. All inputs are protected for transients up to ±50 V. Each counter can be read as well as written from software.

An external Inhibit signal can be used to gate off all counters. Each counter has both an overflow bit and an underflow bit which are set on a carry/borrow from bit 16, and generate interrupts, if enabled. (Counters continue to increment after the overflow condition has occurred.) The resulting eight interrupt source bits can be read and cleared individually or in pairs as the associated counter is cleared. The interrupt source bits are ORed, and a single enable permits an interrupt request to be initiated.

In addition to the eight counter input connectors and the two bridged connectors for the external Inhibit signal, the V620 front panel contains a light emitting diode (LED) indicating that interrupt requests are enabled and a LED indicator for each of the eight interrupt source bits.

The V620 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.



Item	Specification
Number of Channels	4
Input Signals	TTL level
Maximum Clock	20 MHz
Maximum Count Value	65,535 (16 bits)
Input Connector Types	Single-pin LEMO receptacle, shell size 00
Mating Connectors	KineticSystems Model 5910-Z1A
Power Requirements	
+5 V	2.4 A, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-sized VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V620-LA11 4-channel, Up/Down Presettable Counter

Related Products

Model 5857-Axyz Cable—1-contact LEMO to Unterminated
Model 5857-Bxyz Cable—1-contact LEMO to 1-contact LEMO
Model 5857-Hxyz Cable—1-contact LEMO to BNC shielded
Model 5910-Z1A Connector—1-contact LEMO

UNPACKING AND INSTALLATION

The Model V620 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V620 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V620 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the modules right-side ground shield. Refer to FIGURE 1.

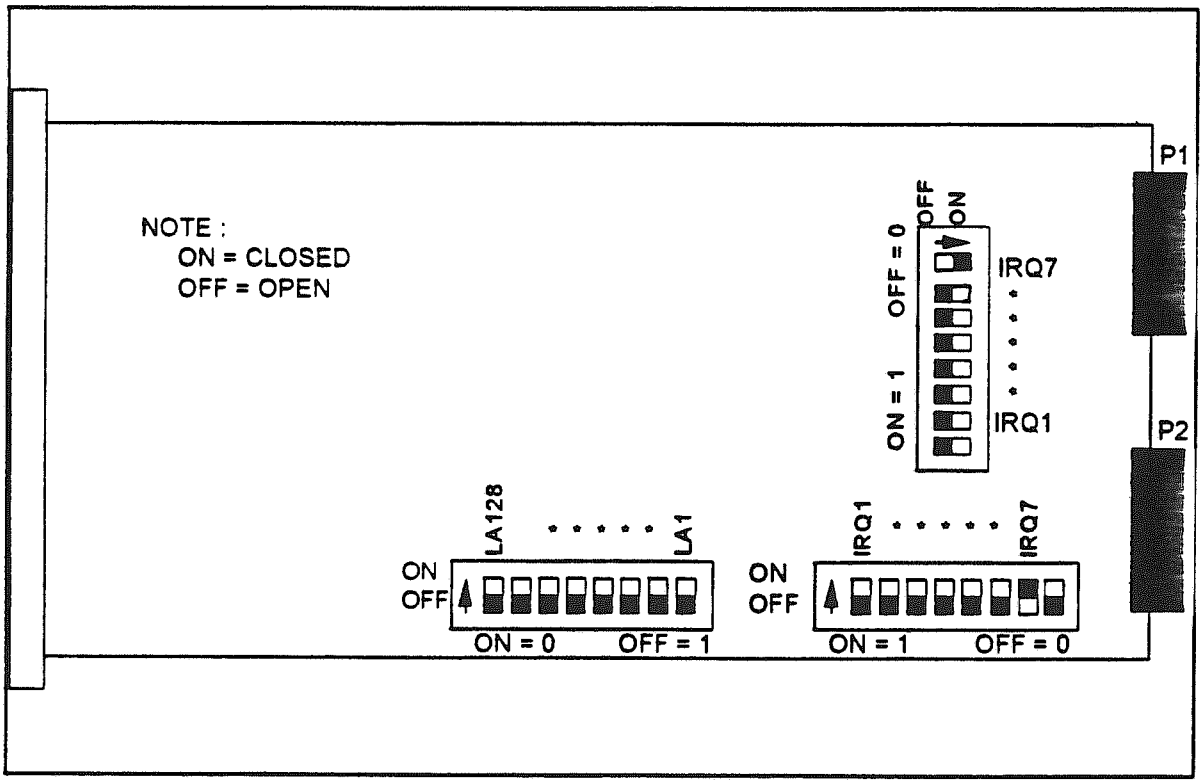


FIGURE 1 - V620 SWITCH LOCATIONS

Model V620-LA11

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to one (VXI defined).
Bits 13 through 6 are user selectable via the address switches LA128-LA1.
Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V620 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 (page 3, 4) for the switch locations and switch settings. Both banks of eight-position switches must be set identical. As shown in Figure 1 (page 3, 4) IRQ 7 is set to the same position in both banks.

Module Insertion

The V620 is a C-sized, single width VXIbus module. It requires 2400 milliamperes of +5 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE

To insure proper interrupt acknowledge cycles from the V620 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Daisy-chain jumpers must be installed in any empty slot between the V620 and the Slot 0 Controller.

FRONT PANEL INFORMATION

LEDs

ADD_REC — This LED turns on when the Operational Registers are being accessed.

INT ENA — This LED turns on when Enable INT Request Register ($4A_{16}$) is read. Likewise, reading Disable INT Request Register ($4E_{16}$) will turn this LED off.

INT SRC — There are eight LEDs that will indicate which interrupt source is set.

CONNECTORS

1-4 UP/DN — These eight single-pin LEMO connectors are the inputs to channels 1 through 4 count UP/DN circuitry. These inputs accept TTL standard Low TRUE signals at the front-panel connector.

I — Two single-pin LEMO connectors are provided to inhibit the counting when a low-true signal is applied. These two connectors are bridged to provide for "Daisy Chaining" with other V620 modules.

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V620 implements those required for register-based devices. The V620 also contains a set of Operational Registers to monitor and control the functional aspects of the devices. Both register sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range (C000 hex to FFFF hex). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of C000 hex to FFC0 hex.

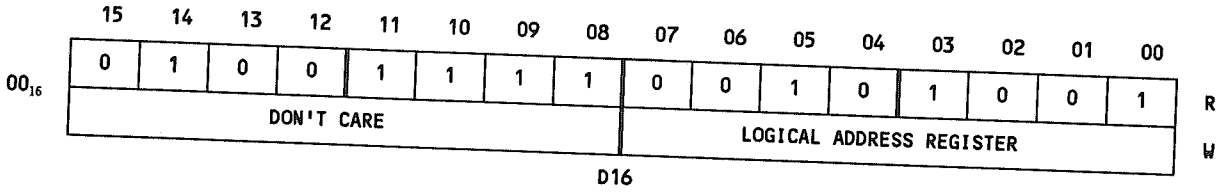
VXIbus Configuration Registers

Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V620 are offset from the base address. Note: The V620 only responds to these addresses if the Short Nonprivileged Access (29 hex) or Short Supervisory Access (2D hex) Address Modifier Codes are set for the backplane bus cycle. Table 1 shows the applicable Configuration Registers present in the V620, their offset from the base (Logical) address, and their Read/Write capabilities.

TABLE 1
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET (HEX)	W/R MODE	REGISTER NAME
00_{16}	W/R	ID/Logical Address Register
02_{16}	R	Device Type Register
04_{16}	W/R	Status/Control Register
06_{16}	W/R	Offset Register
08_{16}	R	Attribute Register
$1E_{16}$	R	Subclass Register

ID/Logical Address Register



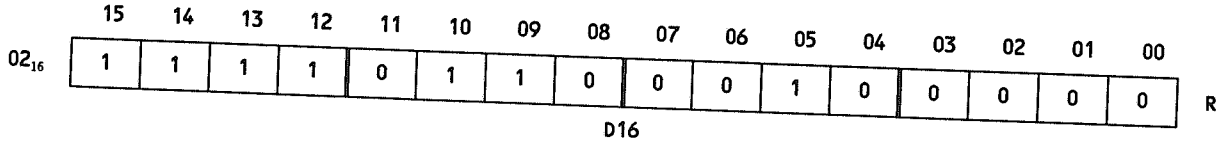
READ

Bits 14,15: Device Class = Extended
Bits 12,13: Address Space = A16/A24 Address Modes
Bits 0-11: Manufacturer ID = KineticSystems ($F29_{16}$)

WRITE

Bits 8-15: Don't Care
Bits 0-7: Logical Address

Device Type



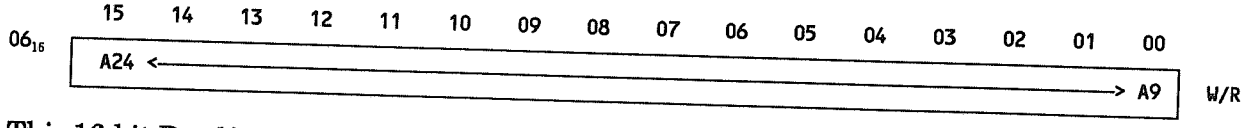
Bits 12-15: Required Memory = 256 Bytes
Bits 0-11: Model Code = 620_{16}

Status/Control Register

15	14	13	12	11 10 09 08 07 06 05 04	03	02	01	00
A24 ACT	MODID	S	1	ZEROS	RDY	PASS	0	RST
A24 ENA	N/U	N/U	1	NOT USED				RST

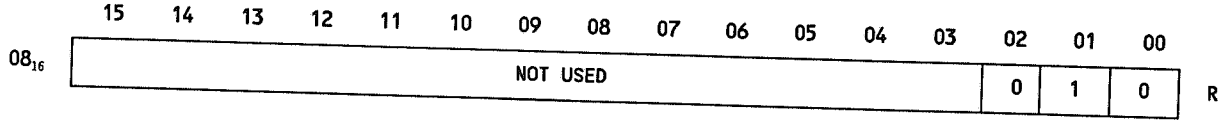
Bit	Mnemonics	Description
15	A24	Writing a one will enable A24 addressing and allow access to the Operational Registers. Reading a one indicates A24 is active. This bit is reset to a zero on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on VXIbus connector P2. A "0" will indicate that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V620. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1".
11-4	N/U	Not used. Read as a zero.
3	RDY	READY. The V620 is always ready. Read as a one.
2	PASS	PASS. The V620 will always pass self tests. Read as a one.
1	N/U	NOT USED. Read as a zero.
0	RST	RESET. This Read/Write bit controls the Soft Reset condition within the V620. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Register (see below), except the Diagnostic and Interrupt Status registers, is inhibited. The Operational Registers are maintained in the state they were in just prior to the Soft Reset being enabled. This bit can be reset by writing a "0", on power-up or the assertion of SYSRESET*.

Offset Register



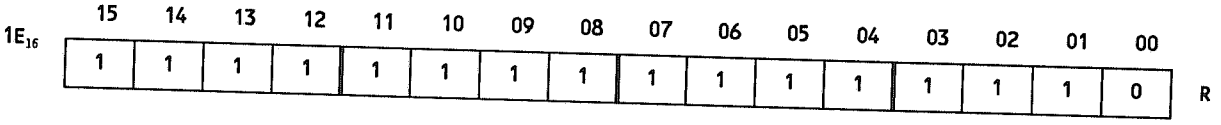
This 16-bit Read/Write register defines the base address of this A24 Operational Register. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Attribute Register



Bits 3-15:	Not Used. Read as zeros
Bit 2 = 0	Indicates Interrupt Control Capability
Bit 1 = 1	Not an Interrupt Handler
Bit 0 = 0	Indicates Interrupt Status Capability

Subclass Register



Bit 15 = 1	Indicates that this is a VXIbus defined Extended Device
Bits 14-0 = $7FFE_{16}$	Indicates that this is an Extended Register Based Device

OPERATIONAL REGISTERS

The Operational Register is your channel to access the functional registers of the V620. For compatibility with other KineticSystems' VXIbus modules in this series, these registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register. Note: The V620 will only respond to these addresses if the Standard Nonprivileged Data Access (39 hex), Standard Nonprivileged Program Access (3A hex), Standard Supervisory Data Access (3D hex), or Standard Supervisory Program Access (3E hex) Address Modifier Codes are set for the bus cycle(s).

Of the 256 bytes requested by the setting of the Device Type Register in the Configuration Register set, only 62 bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type Register.) TABLE 2 shows the applicable Operational

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Registers present in the V620, their offset from the base A24 address, and their Read/Write capabilities.

TABLE 2
V620 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

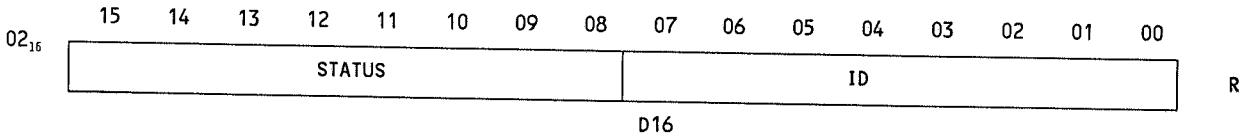
A24 OFFSET	W/R MODE	REGISTER NAME
00_{16}	W/R	Diagnostic Register
02_{16}	W/R	Interrupt Status/ID Register
12_{16}	R	Channel #1
16_{16}	R	Channel #2
$1A_{16}$	R	Channel #3
$1E_{16}$	R	Channel #4
22_{16}	R	Read Channel/Clear INTs #1
26_{16}	R	Read Channel/Clear INTs #2
$2A_{16}$	R	Read Channel/Clear INTs #3
$2E_{16}$	R	Read Channel/Clear INTs #4
32_{16}	W	Channel #1
36_{16}	W	Channel #2
$3A_{16}$	W	Channel #3
$3E_{16}$	W	Channel #4
42_{16}	R	Interrupt Status Register
46_{16}	R	Increment all Channels
$4A_{16}$	R	Decrement all Channels
$4E_{16}$	R	Enable INT Request
52_{16}	R	Disable INT Request
56_{16}	R	Clear Channel / INT Status #1
$5A_{16}$	R	Clear Channel / INT Status #2
$5E_{16}$	R	Clear Channel / INT Status #3
62_{16}	R	Clear Channel / INT Status #4
66_{16}	R	Clear INT Status bit #1
$6A_{16}$	R	Clear INT Status bit #2
$6E_{16}$	R	Clear INT Status bit #3
72_{16}	R	Clear INT Status bit #4
76_{16}	R	Clear INT Status bit #5
$7A_{16}$	R	Clear INT Status bit #6
$7E_{16}$	R	Clear INT Status bit #7
82_{16}	R	Clear INT Status bit #8

Diagnostic Register 00_{16}

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care								D	S	0	INT ENA	INT SRC	0	0	0	R
00_{16}	Don't Care								0	0	0	INT ENA	0	0	CLR	INIT	W
	D16																

Bit	Mnemonic	Description
15-8	D/C	Don't Care.
7	Diagnostic	When this bit is set to a one, the last register access to the Operational Registers (12_{16} through $5E_{16}$) is valid.
6	Status	When this bit is set to a one, the last register access to the Operational Registers (12_{16} through $5E_{16}$) is accepted.
5	N/U	Not Used.
4	INT ENA	Interrupt Enable: Setting this bit to a one will enable interrupts.
3	INT SRC	Interrupt Source: When this bit is set to a one, a channel has either overflowed or underflowed.
2	N/U	Not Used.
1	CLR	Setting this bit will clear the counters and interrupt status bits.
0	INIT	Setting this bit to a one will only reset the Operational Registers (12_{16} through $5E_{16}$). The Configuration Registers and the Diagnostic Registers are unaffected.

Interrupt Status/ID Register 02_{16}



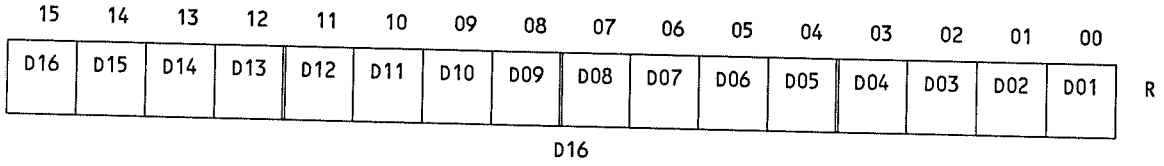
This is a Read-Only 16-bit Interrupt Status Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.

Bit	Mnemonic	Description
15-8	STATUS	These eight bits will indicate Request True or Request False. Request True = FD_{16} Request False = FC_{16}

7-0	ID	These eight bits represent the Logical Address of the V620 Configuration Registers.

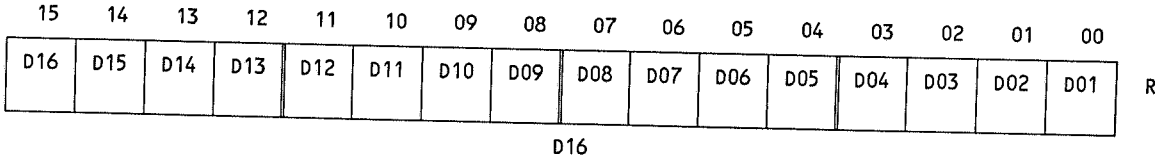
Read Channel Counter Register

A read from the Channel Counter Register will return the current count value for that channel. Channels 1, 2, 3 and 4 are read from registers 12_{16}, 16_{16}, $1A_{16}$ and $1E_{16}$ respectively. The status bit in the Diagnostic Register will always be equal to a one when these registers (12_{16} through $1E_{16}$) are read. Refer to TABLE 2 for the Register Layout on the Channel Counter registers.



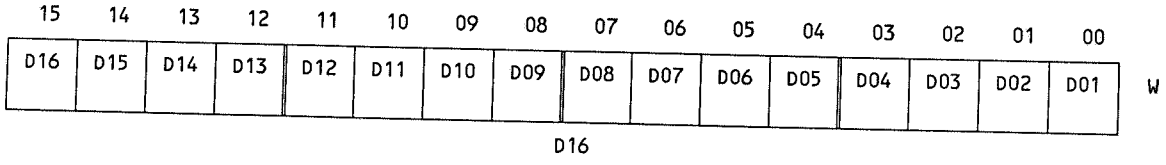
Read & Clear Channel Counter Registers

A read from this register will read the Channel Counter Register and then clear the Counter Register to zero. Channels 1, 2, 3 and 4 are read/cleared from registers 22_{16}, 26_{16}, $2A_{16}$ and $2E_{16}$ respectively. The status bit in the Diagnostic Register will always be equal to a one when these registers (22_{16} through $2E_{16}$) are read. Refer to TABLE 2 for the Register Layout on the Channel Counter Registers.



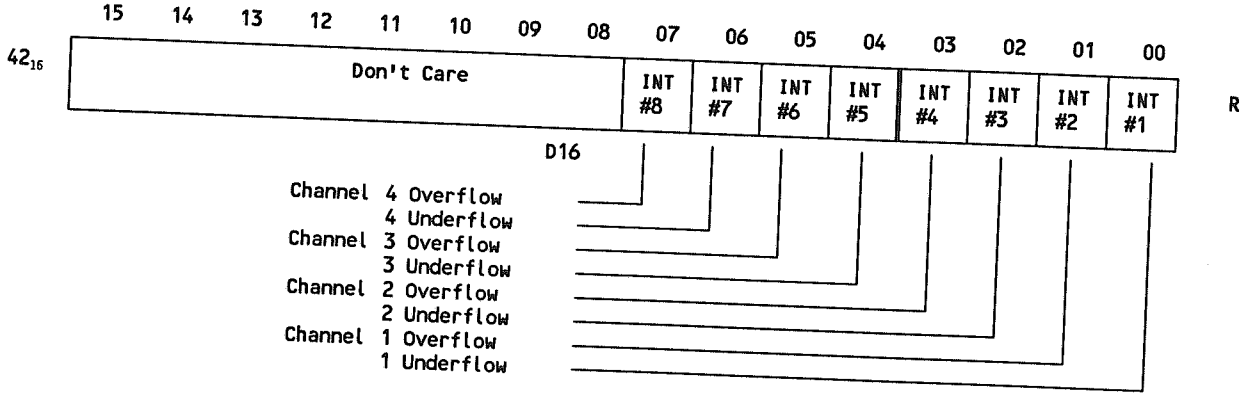
Write Channel Counter Registers

This register is used to load the Channel Count Register. Channels 1, 2, 3 and 4 are loaded by writing to registers 32_{16}, 36_{16}, $3A_{16}$ and $3E_{16}$ respectively. The status bit in the Diagnostic Register will always equal to a one when these registers (32_{16} through $3E_{16}$) are read. Refer to TABLE 2 for the Register Layout on the Channel Counter Registers.



Interrupt Status Register 42_{16}

This register is used to read out the interrupt status bits in the V620. These bits are set to indicate when a channel overflows its counting registers and are used to determine which counter has caused an interrupt. If Interrupt request is enabled, a read from this register will always set the status bit in the Diagnostic Register to a one. A Register Layout is shown below:



OPERATIONAL CONTROL REGISTERS

The V620 has sixteen Operational Control Registers at offset 46_{16} through 82_{16}. These registers are Read-Only and return a 16-bit data code. There are only two possible codes that can be returned. The first data code will return a value of zero and has the same meaning as the Status bit in the Diagnostic Register set to logical "0". The second data code will return a value of one and has the same meaning as the Status bit in the Diagnostic Register set to a logical "1". This data code will indicate the command was accepted or a test condition is true when equal to one. These sixteen Operation Control Registers are described below:

Increment All Channels 46_{16}
Decrement All Channels $4A_{16}$

For every read from either register, one increment or decrement pulse is generated for all channels. This register will always return a data code of one.

Enable INT Request $4E_{16}$
Disable INT Request 52_{16}

A read from either register will enable or disable INT Request. Interrupt Request must be enabled if the V620 is going to set an interrupt. Both registers will return a data code of one.

Clear Channel/INT Status

There are four registers (56_{16} through 62_{16}) to clear each channel individually. When a read operation is preformed to any one of these registers, the Channel Count Register and associated overflow and underflow interrupt status bits for that channel are cleared. These four registers will always return a data code of one.

Clear INT Status

There are eight registers (66_{16} through 82_{16}) to clear each interrupt bit individually. When a Read operation is preformed to any one of these registers, the channel interrupt status bits for that channel are cleared. These eight registers correspond to the eight interrupt status bits in register 42_{16}. These registers will always return a data code of one.

INTERRUPTS

The V620 can generate an interrupt from one of four sources. Each channel can generate an interrupt when the counter overflows or underflows. The counter for a given channel overflows when the count exceeds 65,535 (FFFF hex). When counting down and the counter contains zero, the next down-pulse will set the corresponding underflow interrupt status bit.

The V620 must be setup properly in order to interrupt the VXIbus. First, the interrupt switches must select one of seven Interrupt Requests by switching the appropriate IRQ switches to the "ON" position. Refer to the Interrupt Request Switch Selection for further information. Next, enable interrupt in the following manner:

Enable Interrupt Request by reading the ENA INT Request Register.

Enable Interrupts to the VXIBUS by writing Bit 4 in the Diagnostic Register to a Logical "1".

The V620 is now able to cause an interrupt on the VXIbus. Once the V620 sets an interrupt, an interrupt handler will read the Status/ID Register and reset the Enable Interrupt bit in the Diagnostic Register to a Logical "0". At this time, the interrupt request should be cleared which will also clear INT SRC in the Diagnostic Register to a Logical "0". To clear an Interrupt request, read the Interrupt Status Register to determine which interrupt status bit is causing the interrupt. Then clear the interrupt status bit with the appropriate clear function. Refer to Table 2, V620 Operational Registers, for a list of clear functions. Once INT SRC Bit 3 in the Diagnostic Register is set to a Logical "0", the Interrupt Enable Bit 4 in the Diagnostic Register can be set to a Logical "1". If INT SRC is a Logical "1" when INT ENA is set to a Logical "1", an interrupt will occur instantly.

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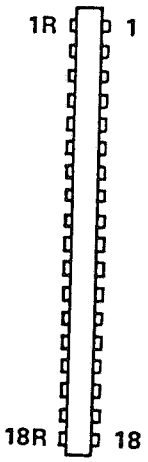

FACE VIEW

V620-LA11 Pin/Wire List

Pin/Wire List

18/36 POSTION P.C. EDGE

PIN NO.	
1R	Module Common
2R	
3R	
4R	
5R	
6R	
7R	
8R	
9R	
10R	
11R	
12R	
13R	
14R	
15R	
16R	
17R	
18R	

PIN NO.	
1	Module Common
2	Channel 4 Up Input
3	Channel 4 Down Input
4	Channel 3 Up Input
5	Channel 3 Down Input
6	Channel 2 Up Input
7	Channel 2 Down Input
8	Channel 1 Up Input
9	Channel 1 Down Input
10	
11	
12	Channel 1 Ext. Clear
13	Channel 2 Ext. Clear
14	Channel 3 Ext. Clear
15	Channel 4 Ext. Clear
16	
17	
18	

ting Connectors: Model 5960, 5961

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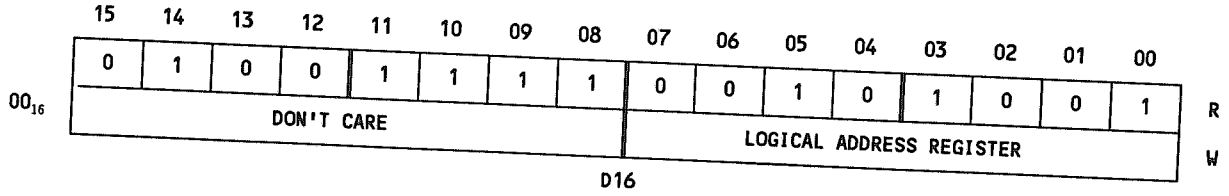
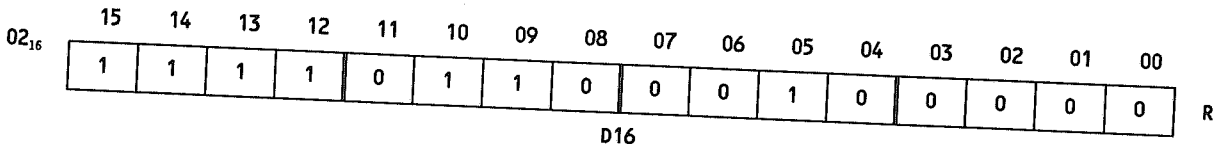
V620 REGISTER LAYOUT

CONFIGURATION REGISTERS

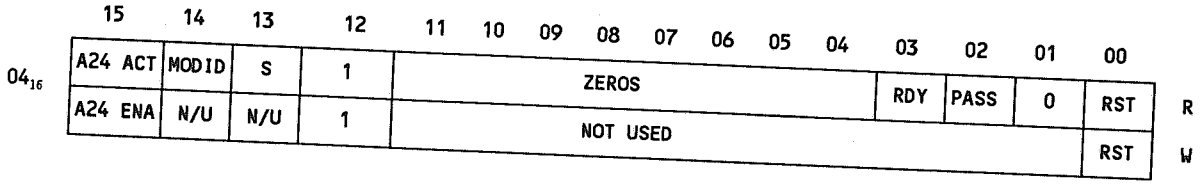
ID/Logical Address Register



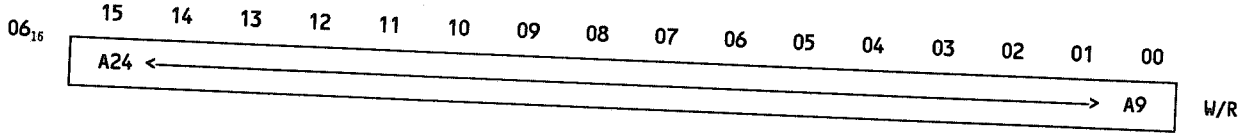
Device Type



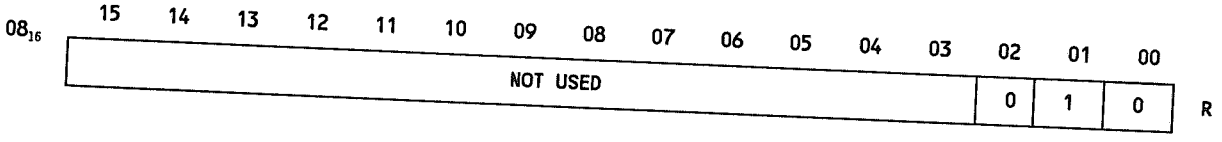
Status/Control Register



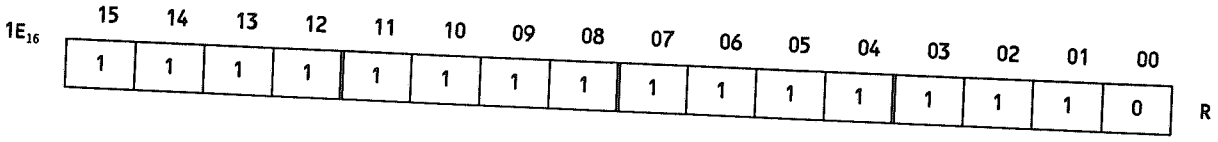
Offset Register



Attribute Register

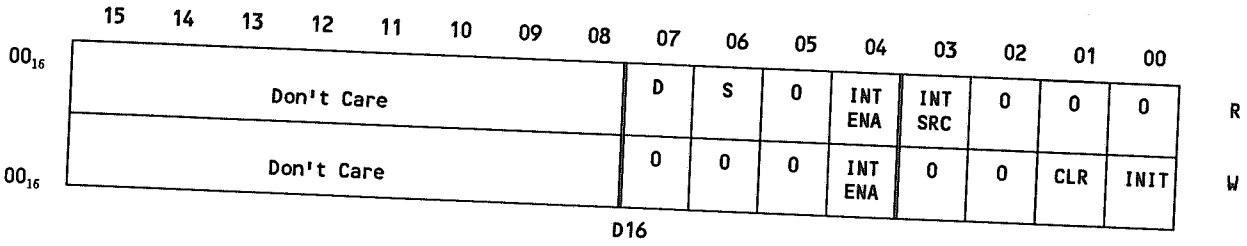


Subclass Register

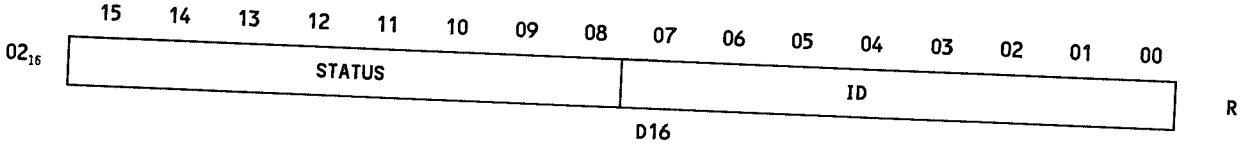


OPERATIONAL REGISTERS

Diagnostic Register

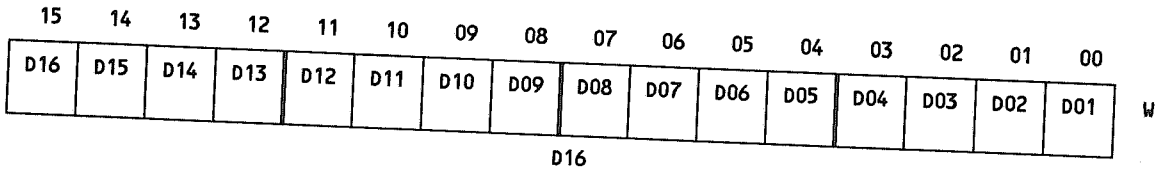


Interrupt Status/ID Register 02

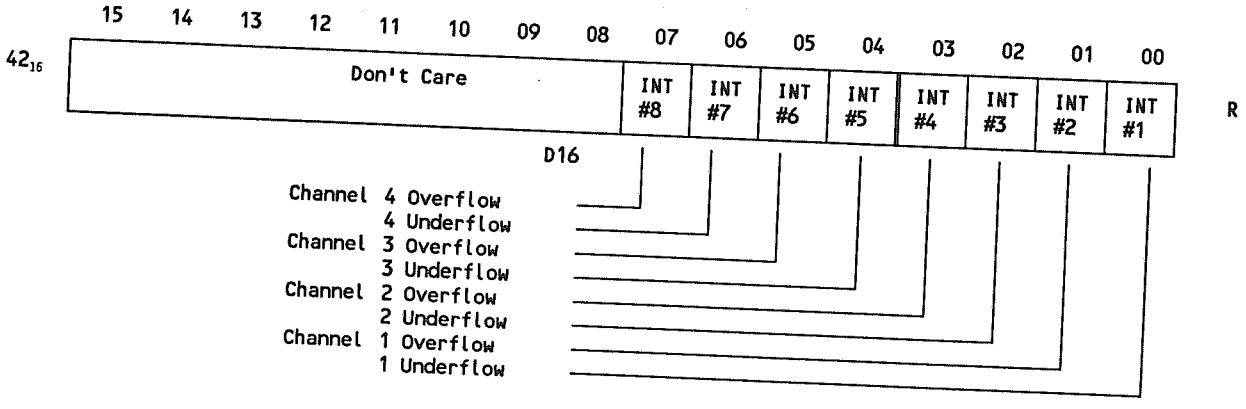


Read Channel Counter Register
Read & Clear Channel Counter Register
Write Channel Counter Register

CH 1-4 12_{16}, 16_{16}, $1A_{16}$, $1E_{16}$
CH 1-4 22_{16}, 26_{16}, $2A_{16}$, $2E_{16}$
CH 1-4 32_{16}, 36_{16}, $3A_{16}$, $3E_{16}$



Interrupt Status Register



OPERATIONAL CONTROL REGISTERS

46_{16}	Increment All Counters
$4A_{16}$	Decrement All Counters
$4E_{16}$	Enable INT Request
52_{16}	Disable INT Request
56_{16}	Clear Channel / INT Status #1
$5A_{16}$	Clear Channel / INT Status #2
$5E_{16}$	Clear Channel / INT Status #3
62_{16}	Clear Channel / INT Status #4
66_{16}	Clear INT Status Bit #1
$6A_{16}$	Clear INT Status Bit #2
$6E_{16}$	Clear INT Status Bit #3
72_{16}	Clear INT Status Bit #4
76_{16}	Clear INT Status Bit #5
$7A_{16}$	Clear INT Status Bit #6
$7E_{16}$	Clear INT Status Bit #7
82_{16}	Clear INT Status Bit #8