Model V625-LA11\LB11

6-Channel Time Interval Counter

INSTRUCTION MANUAL

March, 1998

CONTENTS

Features and Applications 1
General Description 1
Specifications 2
Ordering Information 2

UNPACKING AND INSTALLATION 3
Logical Address Switches 3
Interrupt Switches 4
Module Insertion 4

FRONT PANEL INFORMATION 4
LEDs 4

CONNECTORS 5

PROGRAMMING INFORMATION 5
VMEbus/VXIbus Addressing 5
VXIbus Configuration Registers 5
ID/Logical Address Register 6
Device Type 6
Status/Control Register 7
Offset Register 8
Attribute Register 8
Subclass Register 8

OPERATIONAL REGISTERS 8
Diagnostic Register 10
Interrupt Status/ID Register 10
Time Interval Accumulator Register 11
Read & Clear Accumulator Registers 12
Pulse Counter Registers 13
Interval Timer/Clear Accumulators Register $5A_{16}$ 14
Interrupt Mask Register $5E_{16}$ 14
Interrupt Status Register 62_{16} 15
Operational Control Register 15
Initiate Timing Cycle on All Channels 66_{16} 15

INTERRUPTS 16

V625 REGISTER LAYOUT 18-21

FIGURES

FIGURE 1 - V625 SWITCH LOCATIONS 3

TABLES

TABLE 1 - CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE 6
TABLE 2 - V625 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE 9

WARRANTY
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6-channel Time Interval Counter

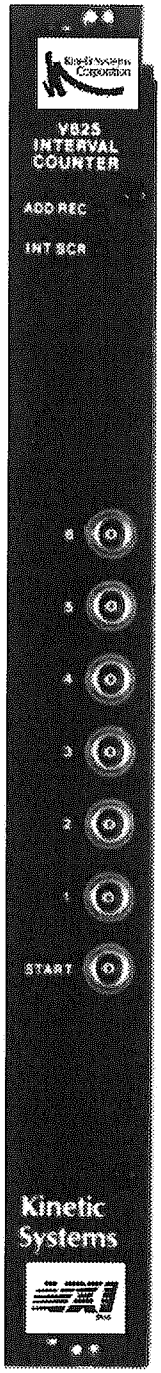
Measures the intervals from a common start pulse to 6 stop pulses **V625**

Features

- **6-channel capacity**
- **TTL and optically-isolated input options**
- **8 clock frequencies (1 Hz to 10 MHz)**
- **16-bit pulse counters per channel (max count=65,535)**
- **24-bit time interval counters per channel (16,777,215)**
- **Individual interrupt source bit per channel**

Typical Applications

- **Test cells**
- **Nuclear accelerator control and monitoring**
- **General-purpose time interval measurement**



General Description *(Product specifications and descriptions subject to change without notice.)*

The V625 is a single-width, C-size, register-based, VXIbus module that contains six channels of time interval counters. Data from the module can be used to represent the time elapsed between a Start and a Stop pulse, or it can be used to determine the average frequency of an input pulse train. Each channel contains a 24-bit time interval accumulator and a 16-bit, presettable input pulse counter. Latches are provided to hold the pulse count, thereby eliminating the need to continuously rewrite the count value. Time intervals are derived from a common, crystal-controlled clock on the module. The clock frequency is software programmable, and can range from 1 Hz to 10 MHz, in decade steps. Once the timing cycle has been initiated (by a software command or front-panel input signal), the accumulators record timing information until the preset number of input pulses has been received by the V625. The overflow from each channel's input pulse counter or time interval accumulator stops the timing sequence for that channel and sets an interrupt source bit. An interrupt Mask register allows any source bit or combination of bits to generate an interrupt request.

The common Start signal and the six pulse inputs are connected to the module's circuitry via single-pin LEMO connectors on the module's front panel. The Start signal is a low-true, TTL pulse which initiates the timing cycle on the low-to-high transition. By order option, the pulse inputs are either TTL-level signals or optically-isolated, 10 V pulses supplying 15 mA of drive current. The maximum frequency of the input pulses is 5 MHz, and the counter chains are incremented on the low-to-high transition of each pulse.

The V625 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.

V625 *(continued)*

Item	Specification
Number of Channels	6
Input Signals	TTL-level or optically-isolated, 10 V, 15 mA signals
Pulse Inputs	
Input-output insulation	1μA, with 45% relative humidity, t = 5s, V_{I-O} = 3 kV dc, T_A = 25°C
Input-output resistance	10^{12} Ω
Maximum Input Pulse Rate	5 MHz with a 50% duty cycle
Time Interval Clock	
Source	Crystal-controlled, common to all channels
Frequency choices (programmable)	1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz
Crystal Source	
Overall stability	±0.01%, 0°C to +70°C
Maximum Count Value	
Input pulse counter chain	65,535 (16 bits)
Time interval accumulators	16,777,215 (24 bits)
Input Connector Types	Single-pin LEMO receptacle, shell size 00
Mating Connectors	KineticSystems Model 5910-Z1A
Power Requirements	
+5 V	3.2 A, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-sized VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V625-LA11 6-channel Time Interval Counter, TTL Inputs
Model V625-LB11 6-channel Time Interval Counter, Optically-isolated Inputs

Related Products

Model 5857-Axyz Cable—1-contact LEMO to Unterminated
Model 5857-Bxyz Cable—1-contact LEMO to 1-contact LEMO
Model 5857-Hxyz Cable—1-contact LEMO to BNC shielded
Model 5910-Z1A Connector—1-contact LEMO

UNPACKING AND INSTALLATION

The Model V625 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V625 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V625 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the modules right-side ground shield. Refer to FIGURE 1.

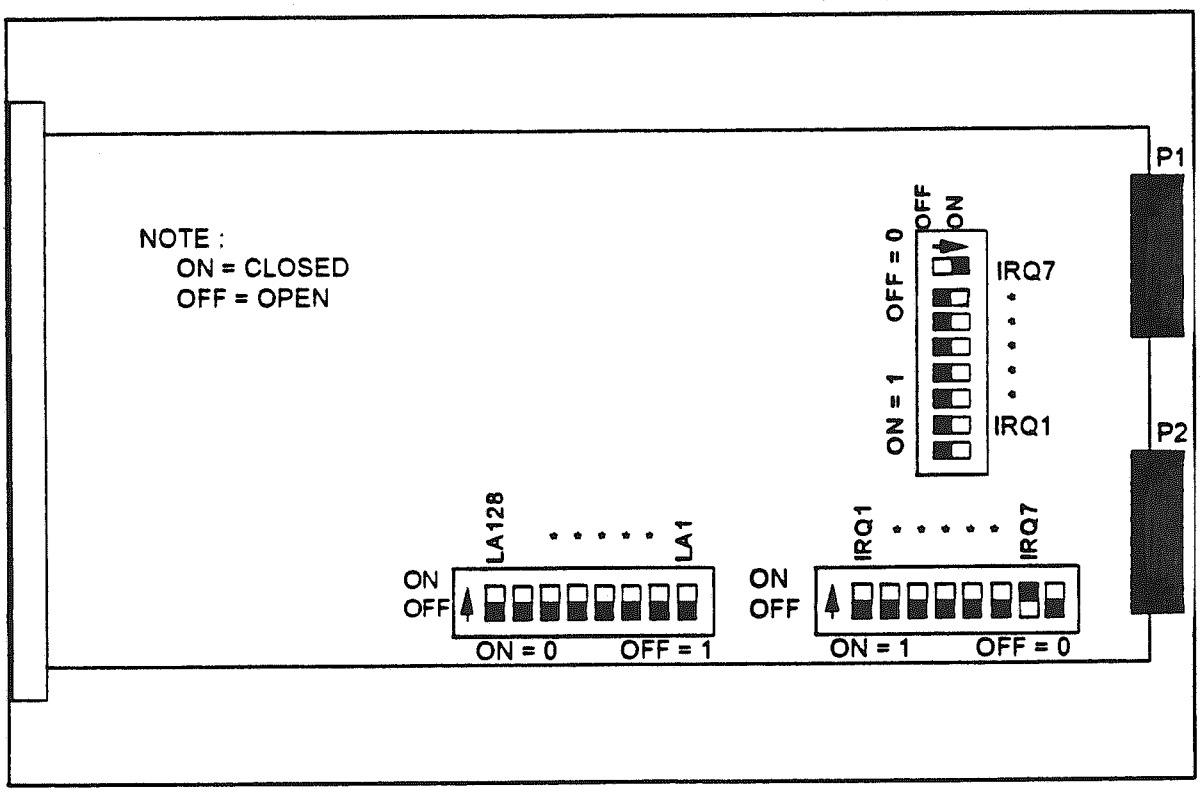


FIGURE 1 - V625 SWITCH LOCATIONS

Model V625-LA11\LB11

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to one (VXI defined).
Bits 13 through 6 are user selectable via the address switches LA128-LA1.
Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V625 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 (page 3) for the switch locations and switch settings. Both banks of eight-position switches must be set identical. As shown in Figure 1 (page 3) IRQ 7 is set to the same position in both banks.

Module Insertion

The V625 is a C-sized, single width VXIbus module. It requires 3200 milliamperes of +5 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE

To insure proper interrupt acknowledge cycles from the V625 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Daisy-chain jumpers must be installed in any empty slot between the V625 and the Slot 0 Controller.

FRONT PANEL INFORMATION

LEDs

ADD_REC — This LED turns on when the Operational Registers are being accessed.

INT SRC — This LED turns on when any one of the six channels has set its interrupt status bit.

CONNECTORS

1-6	These six single-pin LEMO connectors are the pulse inputs to channels 1 through 6. The pulse inputs are TTL level signals. The maximum frequency of the input pulses is five megahertz, and the counter chains are incremented on the low-to-high transition of each pulse.
Start	This single-pin LEMO connector is the common Start signal for the six pulse inputs. The Start signal is a low-true, TTL pulse which initiates the timing cycle on a low-to-high transition.

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V625 implements those required for register-based devices. The V625 also contains a set of Operational Registers to monitor and control the functional aspects of the devices. Both register sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range (C000 hex to FFFF hex). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of C000 hex to FFC0 hex.

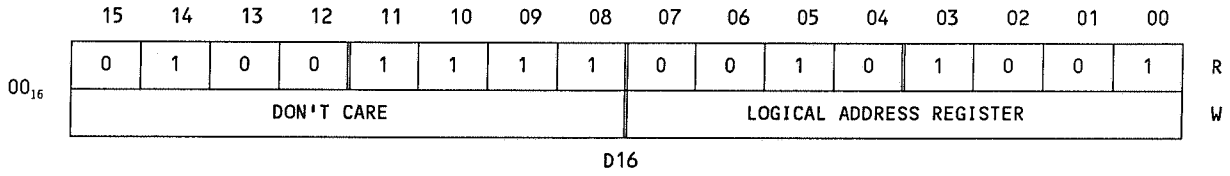
VXIbus Configuration Registers

Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V625 are offset from the base address. Note: The V625 only responds to these addresses if the Short Nonprivileged Access (29 hex) or Short Supervisory Access (2D hex) Address Modifier Codes are set for the backplane bus cycle. Table 1 shows the applicable Configuration Registers present in the V625, their offset from the base (Logical) address, and their Read/Write capabilities.

TABLE 1
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET (HEX)	W/R MODE	REGISTER NAME
00_{16}	W/R	ID/Logical Address Register
02_{16}	R	Device Type Register
04_{16}	W/R	Status/Control Register
06_{16}	W/R	Offset Register
08_{16}	R	Attribute Register
$1E_{16}$	R	Subclass Register

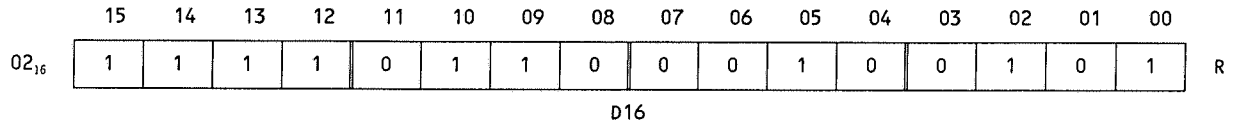
ID/Logical Address Register



READ
Bits 14,15: Device Class = Extended
Bits 12,13: Address Space = A16/A24 Address Modes
Bits 0-11: Manufacturer ID = KineticSystems ($F29_{16}$)

WRITE
Bits 8-15: Don't Care
Bits 0-7: Logical Address

Device Type



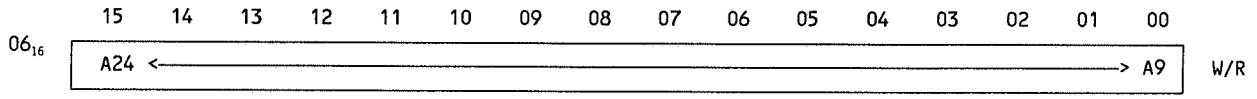
Bits 12-15: Required Memory = 256 Bytes
Bits 0-11: Model Code = 625_{16}

Status/Control Register

15	14	13	12	11 10 09 08 07 06 05 04	03	02	01	00	
A24 ACT	MODID	S	1	ZEROS	RDY	PASS	0	RST	R
A24 ENA	N/U	N/U	1	NOT USED				RST	W

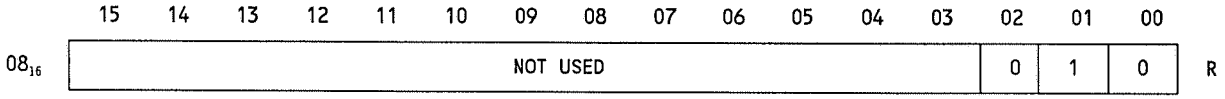
Bit	Mnemonics	Description
15	A24	Writing a one will enable A24 addressing and allow access to the Operational Registers. Reading a one indicates A24 is active. This bit is reset to a zero on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on VXIbus connector P2. A "0" will indicate that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V625. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1".
11-4	N/U	Not used. Read as a zero.
3	RDY	READY. The V625 is always ready. Read as a one.
2	PASS	PASS. The V625 will always pass self tests. Read as a one.
1	N/U	NOT USED. Read as a zero.
0	RST	RESET. This Read/Write bit controls the Soft Reset condition within the V625. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Register (see below), except the Diagnostic and Interrupt Status registers, is inhibited. The Operational Registers are maintained in the state they were in just prior to the Soft Reset being enabled. This bit can be reset by writing a "0", on power-up or the assertion of SYSRESET*.

Offset Register



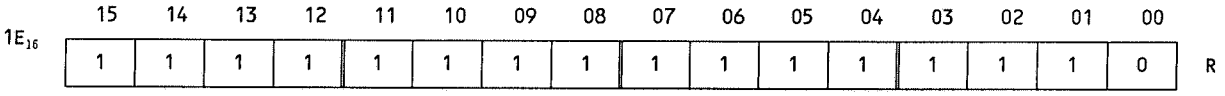
This 16-bit Read/Write register defines the base address of this A24 Operational Register. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Attribute Register



Bits 3-15: Not Used. Read as zeros
Bit 2 = 0 Indicates Interrupt Control Capability
Bit 1 = 1 Not an Interrupt Handler
Bit 0 = 0 Indicates Interrupt Status Capability

Subclass Register



Bit 15 = 1 Indicates that this is a VXIbus defined Extended Device
Bits 14-0 = $7FFE_{16}$ Indicates that this is an Extended Register Based Device

OPERATIONAL REGISTERS

The Operational Register is your channel to access the functional registers of the V625. For compatibility with other KineticSystems' VXIbus modules in this series, these registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register. Note: The V625 will only respond to these addresses if the Standard Nonprivileged Data Access (39 hex), Standard Nonprivileged Program Access (3A hex), Standard Supervisory Data Access (3D hex), or Standard Supervisory Program Access (3E hex) Address Modifier Codes are set for the bus cycle(s).

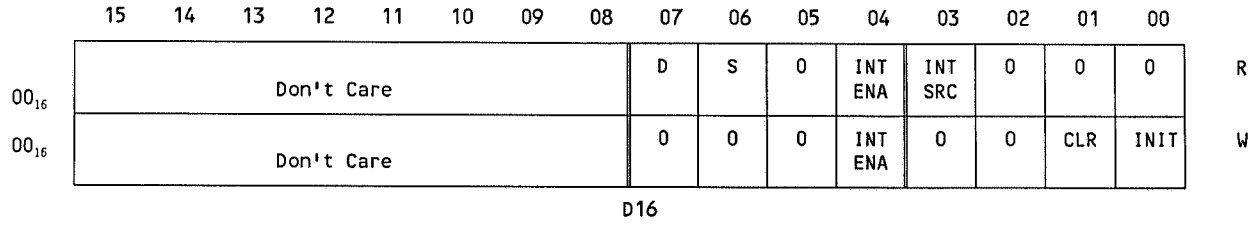
Of the 256 bytes requested by the setting of the Device Type Register in the Configuration Register set, only 72 bytes are used. (256 is the minimum number of bytes that can be

requested through the Device Type Register.) TABLE 2 shows the applicable Operational Registers present in the V625, their offset from the base A24 address, and their Read/Write capabilities.

TABLE 2
V625 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

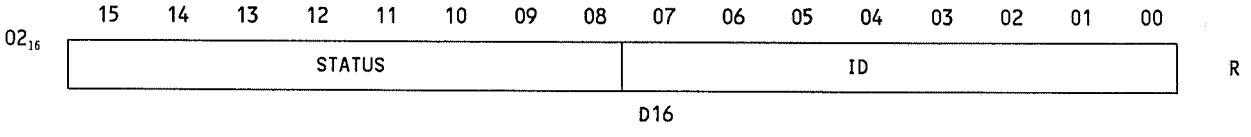
A24 OFFSET	W/RMODE	REGISTER NAME
00_{16}	W/R	Diagnostic Register
02_{16}	W/R	Interrupt Status/ID Register
12_{16}	R	Channel #1 Time Interval Accumulator Low
14_{16}	R	Channel #1 Time Interval Accumulator High
16_{16}	R	Channel #2 Time Interval Accumulator Low
18_{16}	R	Channel #2 Time Interval Accumulator High
$1A_{16}$	R	Channel #3 Time Interval Accumulator Low
$1C_{16}$	R	Channel #3 Time Interval Accumulator High
$1E_{16}$	R	Channel #4 Time Interval Accumulator Low
20_{16}	R	Channel #4 Time Interval Accumulator High
22_{16}	R	Channel #5 Time Interval Accumulator Low
24_{16}	R	Channel #5 Time Interval Accumulator High
26_{16}	R	Channel #6 Time Interval Accumulator Low
28_{16}	R	Channel #6 Time Interval Accumulator High
$2A_{16}$	R	Read & Clear Accumulator Channel #1 Low/INT #1
$2C_{16}$	R	Read & Clear Accumulator Channel #1 High/INT #1
$2E_{16}$	R	Read & Clear Accumulator Channel #2 Low/INT #2
30_{16}	R	Read & Clear Accumulator Channel #2 High/INT #2
32_{16}	R	Read & Clear Accumulator Channel #3 Low/INT #3
34_{16}	R	Read & Clear Accumulator Channel #3 High/INT #3
36_{16}	R	Read & Clear Accumulator Channel #4 Low/INT #4
38_{16}	R	Read & Clear Accumulator Channel #4 High/INT #4
$3A_{16}$	R	Read & Clear Accumulator Channel #5 Low/INT #5
$3C_{16}$	R	Read & Clear Accumulator Channel #5 High/INT #5
$3E_{16}$	R	Read & Clear Accumulator Channel #6 Low/INT #6
40_{16}	R	Read & Clear Accumulator Channel #6 High/INT #6
42_{16}	W	Channel #1 Pulse Counter
46_{16}	W	Channel #2 Pulse Counter
$4A_{16}$	W	Channel #3 Pulse Counter
$4E_{16}$	W	Channel #4 Pulse Counter
52_{16}	W	Channel #5 Pulse Counter
56_{16}	W	Channel #6 Pulse Counter
$5A_{16}$	W	Interval Timer/Clear Accumulators
$5E_{16}$	W	Interrupt Mask Register
62_{16}	R	Interrupt Status Register
66_{16}	R	Initiates the timing cycle for all channels

Diagnostic Register 00_{16}



Bit	Mnemonic	Description
15-8	D/C	Don't Care.
7	Diagnostic	When this bit is set to a one, the last register access to the Operational Registers (12_{16} through 66_{16}) is valid.
6	Status	When this bit is set to a one, the last register access to the Operational Registers (12_{16} through 66_{16}) is accepted.
5	N/U	Not Used.
4	INT ENA	Interrupt Enable: Setting this bit to a one will enable interrupts.
3	INT SRC	Interrupt Source: When this bit is set to a one, the V625 has overflowed one of the input pulse counters or one of the time interval accumulators.
2	N/U	Not Used.
1	CLR	Setting this bit will clear the counters and interrupt status bits.
0	INIT	Setting this bit to a one will only reset the Operational Registers (12_{16} through 66_{16}). The Configuration Registers and the Diagnostic Registers are unaffected.

Interrupt Status/ID Register 02_{16}



This is a Read-Only 16-bit Interrupt Status Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.

Bit	Mnemonic	Description
15-8	STATUS	These eight bits will indicate Request True or Request False. Request True = FD_{16} Request False = FC_{16}
7-0	ID	These eight bits represent the Logical Address of the V625 Configuration Registers.

Time Interval Accumulator Register

These registers represent the 24-bit time interval that has been accumulated from the start (initiated by either a read of register 66_{16} or by an externally applied pulse to the start LEMO), until the desired number of pulses (loaded in the Pulse Counter Register) have been counted. To read all 24-bits from a Time Interval Accumulator Register, a read from the LOW register must be executed first, followed by a read from the HIGH register. The Low register will return bits one through 16, while the High register will return bits 17 through 24 of the Time Interval Accumulator register. The status bit in the Diagnostic Register will always be equal to a one when these registers (12_{16} through 28_{16}) are read. A Register Layout is shown below:

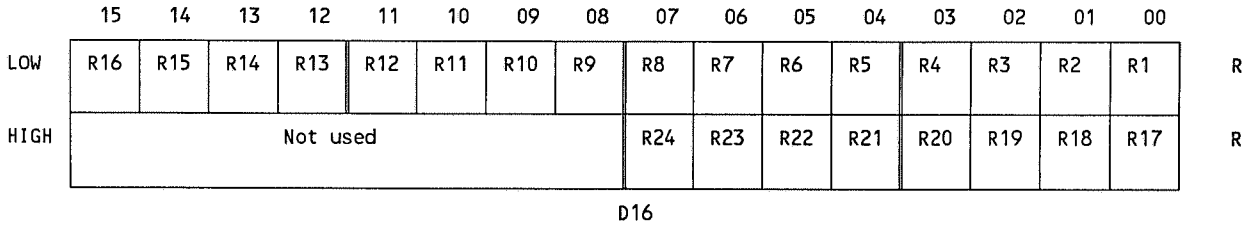
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
LOW	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
HIGH	Not used								R24	R23	R22	R21	R20	R19	R18	R17	R

D16

A24 OFFSET	W/R MODE	REGISTER NAME
12_{16}	R	Channel #1 Time Interval Accumulator Low
14_{16}	R	Channel #1 Time Interval Accumulator High
16_{16}	R	Channel #2 Time Interval Accumulator Low
18_{16}	R	Channel #2 Time Interval Accumulator High
$1A_{16}$	R	Channel #3 Time Interval Accumulator Low
$1C_{16}$	R	Channel #3 Time Interval Accumulator High
$1E_{16}$	R	Channel #4 Time Interval Accumulator Low
20_{16}	R	Channel #4 Time Interval Accumulator High
22_{16}	R	Channel #5 Time Interval Accumulator Low
24_{16}	R	Channel #5 Time Interval Accumulator High
26_{16}	R	Channel #6 Time Interval Accumulator Low
28_{16}	R	Channel #6 Time Interval Accumulator High

Read & Clear Accumulator Registers

A read from these registers will read all 24-bits from a Time Interval Accumulator Register and then clear the Interval Accumulator Register to zero. This operation will also clear the Interrupt status bit associated with a given channel. To read all 24-bits of the Interval Accumulator Register, a read from the LOW register must be executed first, followed by a read from the HIGH register. The Low register will return bits one through 16, while the High register will return bits 17 through 24 of the Time Interval Accumulator register. The status bit in the Diagnostic Register will always be equal to a one when these registers ($2A_{16}$ through 40_{16}) are read. A Register Layout is shown below:



A24 OFFSET	W/R MODE	REGISTER NAME
$2A_{16}$	R	Read & Clear Accumulator Channel #1 Low/INT #1
$2C_{16}$	R	Read & Clear Accumulator Channel #1 High/INT #1
$2E_{16}$	R	Read & Clear Accumulator Channel #2 Low/INT #2
30_{16}	R	Read & Clear Accumulator Channel #2 High/INT #2
32_{16}	R	Read & Clear Accumulator Channel #3 Low/INT #3
34_{16}	R	Read & Clear Accumulator Channel #3 High/INT #3
36_{16}	R	Read & Clear Accumulator Channel #4 Low/INT #4
38_{16}	R	Read & Clear Accumulator Channel #4 High/INT #4
$3A_{16}$	R	Read & Clear Accumulator Channel #5 Low/INT #5
$3C_{16}$	R	Read & Clear Accumulator Channel #5 High/INT #5
$3E_{16}$	R	Read & Clear Accumulator Channel #6 Low/INT #6
40_{16}	R	Read & Clear Accumulator Channel #6 High/INT #6

Pulse Counter Registers

A write to this register loads a channel with the number of input pulses over which time increments are to be accumulated and clears the Time Interval Accumulator. The status bit in the Diagnostic Register will always equal a one when these registers (42_{16} through 56_{16}) are read. A Register Layout is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	W
								D16								

A24 OFFSET	W/R MODE	REGISTER NAME
42_{16}	W	Channel #1 Pulse Counter
46_{16}	W	Channel #2 Pulse Counter
$4A_{16}$	W	Channel #3 Pulse Counter
$4E_{16}$	W	Channel #4 Pulse Counter
52_{16}	W	Channel #5 Pulse Counter
56_{16}	W	Channel #6 Pulse Counter

Interval Timer/Clear Accumulators Register $5A_{16}$

This register is used to select one of eight timing clock frequencies (10^0-10^7 hertz) and clears all Time Interval Accumulators and Interrupt Status bits. If the Time Interval Accumulator overflows before the Pulse Counter overflows, an **ERROR** condition exists indicating that the frequency selected is too fast. The Interrupt Status bit will be set and pulse counting will be diabled. Default frequency after Reset is one hertz. A Register Layout is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	CLK 3	CLK 2	CLK 1	R
D16																

BIT 2 1 0

CLK 3	CLK 2	CLK 1	FREQUENCY (HERTZ)
0	0	0	1 Hz
0	0	1	10 Hz
0	1	0	100 Hz
0	1	1	1 KHz
1	0	0	10 KHz
1	0	1	100 KHz
1	1	0	1 MHz
1	1	1	10 MHz

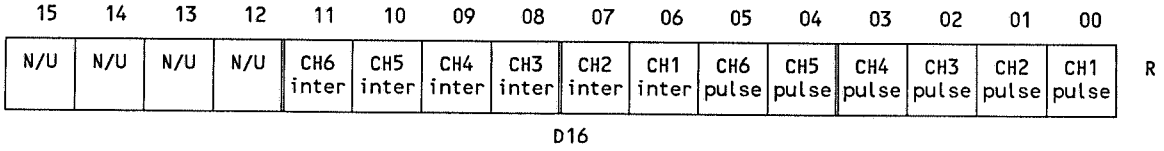
Interrupt Mask Register $5E_{16}$

This register is used to select which channels are able to set the INT SRC (Interrupt Source) bit in the Diagnostic register. Writing a one to the appropriate channels's mask bit (Pulse Counter Overflow or Interval Accumulator Overflow) will cause that channel to set the INT SRC bit upon Overflow. A Register Layout is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
N/U	N/U	N/U	N/U	CH6 inter	CH5 inter	CH4 inter	CH3 inter	CH2 inter	CH1 inter	CH6 pulse	CH5 pulse	CH4 pulse	CH3 pulse	CH2 pulse	CH1 pulse	W
D16																

Interrupt Status Register 62_{16}

This register is used to read out the interrupt status bits in the V625. The lower six bits (0-5) are set to a one when a channel's pulse counter overflows, indicating the desired number of pulses have been counted. The remaining bits (6-11) are set to a one to indicate that an Interval Accumulator overflowed before pulse counting was completed. This is an ERROR condition and indicates that the internal clock speed is set to fast. If the corresponding Interrupt Mask Bit is set, and the INT ENA bit (bit 4) in the Diagnostic Register is set an Interrupt will be generated. A read from this register will always set the status bit in the Diagnostic Register to a one. A Register Layout is shown below:

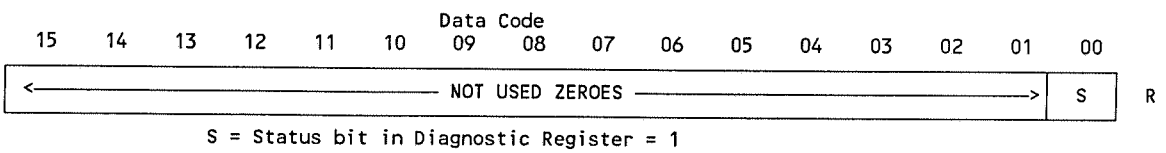


Operational Control Register

The V625 has one Operational Control Register at offset 66_{16}. This register is Read-Only and returns a 16-bit data code. This code has the same menaing as the Status bit in the Diagnostic Register.

Initiate Timing Cycle on All Channels 66_{16}

A read from this register will start the module counting the input pulses on all six channels. Counting will continue until the pulse counter overflows or the Interval Accumulator overflows setting the appropriate Interrupt Status bit and disabling pulse counting. Once all channels have finished counting, another timing cycle can be initiated with the start pulse without having to rewrite the overflow count. If the pulse overflow count is to be changed to a new overflow count, a write to the pulse counter register must be used prior to the start command. The timing data may be read from the Time Interval Accumulators by using the appropriate read or read and clear register. This register always returns a data code of one.



Application Notes: If using the V625 to determine the average frequency of an input pulse train, and the applied input pulse train is a free running clock that is asynchronous with reapect to the mudule's start pulse, one can expect to see a slightly different count returned for several samples of the pulse train. When using the V625 to determine the elasped time between a start and a stop pulse, note that on the falling edge of the start pulse there is a one microsecond delay time to allow the Time Interval Accumulator timing frequency to synchronize with the start pulse. Also note that the pulse counting will be disabled when the Input receives a complete pulse. for example, if the Input pulse is a high true pulse, then the pulse counter will increment on the low-to-high transition, with overflow and pulse counting disable occuring on the high to low transition of that pulse.

INTERRUPTS

The V625 can generate an interrupt from one of six sources. Each channel can generate an interrupt when the Interval Accumulator overflows before the Pulse Counter overflows or the Pulse Counter overflows.
The V625 must be setup properly in order to interrupt the VXIbus. First, the interrupt switches must select one of seven Interrupt Requests by switching the appropriate IRQ switches to the "ON" position. Refer to the Interrupt Request Switch Selection for further information. Next, enable interrupts in the following manner:

Write the Interrupt Mask Register to enable the appropriate source.

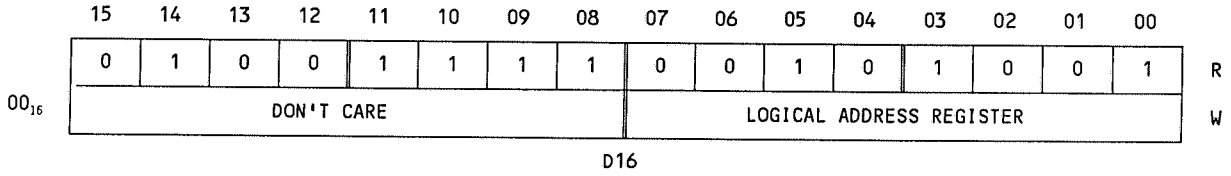
Enable Interrupts to the VXIBUS by writing Bit 4 in the Diagnostic Register to a Logical "1".

The V625 is now able to cause an interrupt on the VXIbus. Once the V625 sets an interrupt, an interrupt handler will read the Status/ID Register and reset the Enable Interrupt bit in the Diagnostic Register to a Logical "0". At this time, the interrupt request should be cleared which will also clear INT SRC in the Diagnostic Register to a Logical "0". To clear an Interrupt request, read the Interrupt Status Register to determine which interrupt status bit is causing the interrupt. Then clear the interrupt status bit by writing/reading the appropriate register as described in Table 2. Once INT SRC Bit 3 in the Diagnostic Register is set to a Logical "0", the Interrupt Enable Bit 4 in the Diagnostic Register can be set to a Logical "1". If INT SRC is a Logical "1" when INT ENA is set to a Logical "1", an interrupt will occur instantly.

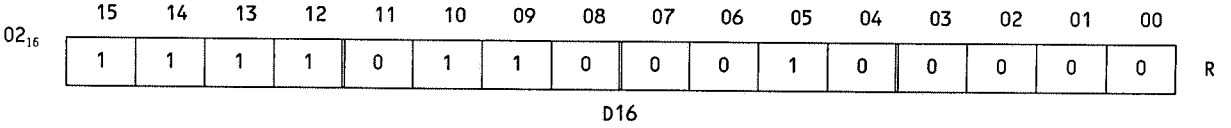
V625 REGISTER LAYOUT

CONFIGURATION REGISTERS

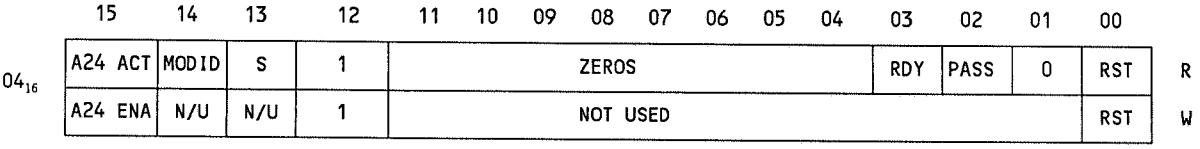
ID/Logical Address Register



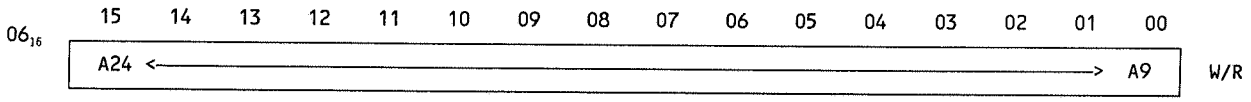
Device Type



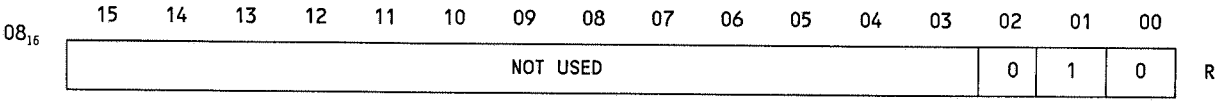
Status/Control Register



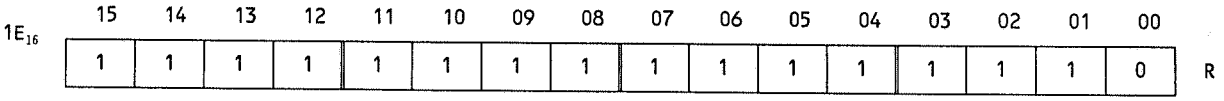
Offset Register



Attribute Register

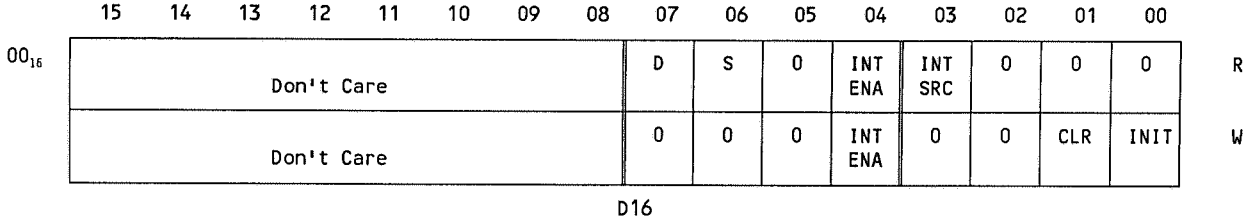


Subclass Register

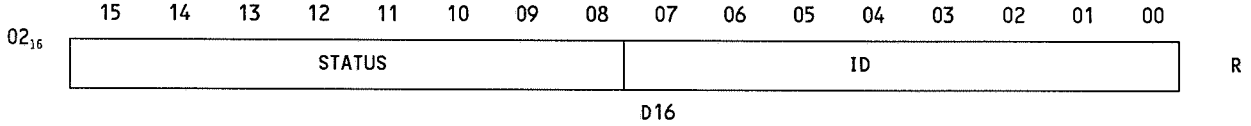


OPERATIONAL REGISTERS

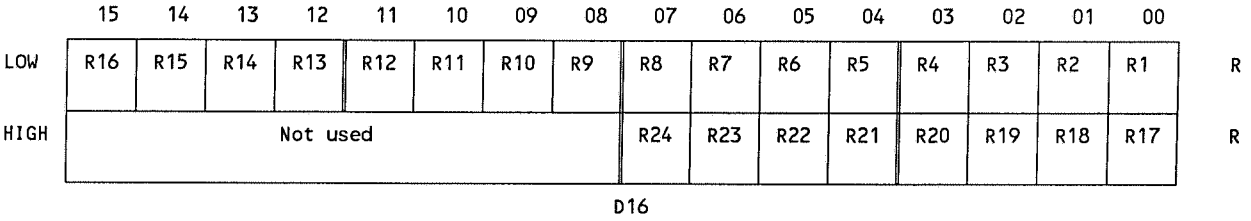
Diagnostic Register



Interrupt Status/ID Register 02_{16}

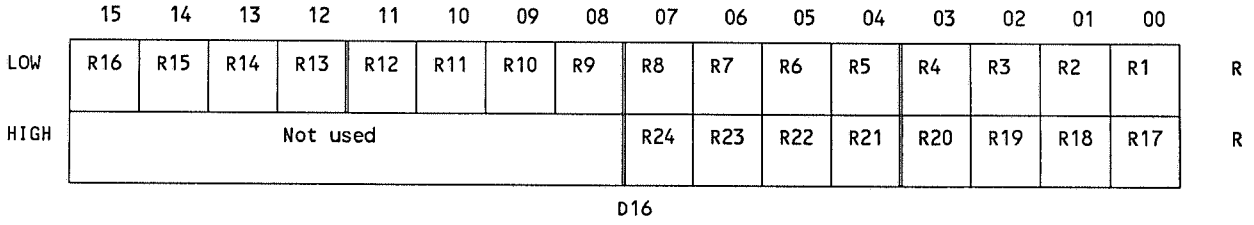


Time Interval Accumulator Register



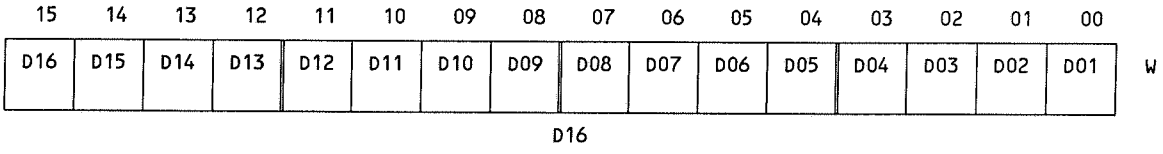
A24 OFFSET	W/R MODE	REGISTER NAME
12_{16}	R	Channel #1 Time Interval Accumulator Low
14_{16}	R	Channel #1 Time Interval Accumulator High
16_{16}	R	Channel #2 Time Interval Accumulator Low
18_{16}	R	Channel #2 Time Interval Accumulator High
$1A_{16}$	R	Channel #3 Time Interval Accumulator Low
$1C_{16}$	R	Channel #3 Time Interval Accumulator High
$1E_{16}$	R	Channel #4 Time Interval Accumulator Low
20_{16}	R	Channel #4 Time Interval Accumulator High
22_{16}	R	Channel #5 Time Interval Accumulator Low
24_{16}	R	Channel #5 Time Interval Accumulator High
26_{16}	R	Channel #6 Time Interval Accumulator Low
28_{16}	R	Channel #6 Time Interval Accumulator High

Read & Clear Accumulator Registers



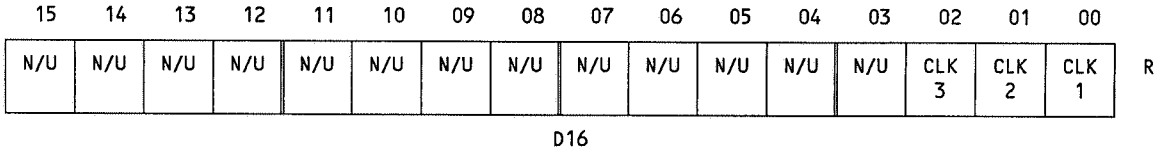
A24 OFFSET	W/R MODE	REGISTER NAME
$2A_{16}$	R	Read & Clear Accumulator Channel #1 Low/INT #1
$2C_{16}$	R	Read & Clear Accumulator Channel #1 High/INT #1
$2E_{16}$	R	Read & Clear Accumulator Channel #2 Low/INT #2
30_{16}	R	Read & Clear Accumulator Channel #2 High/INT #2
32_{16}	R	Read & Clear Accumulator Channel #3 Low/INT #3
34_{16}	R	Read & Clear Accumulator Channel #3 High/INT #3
36_{16}	R	Read & Clear Accumulator Channel #4 Low/INT #4
38_{16}	R	Read & Clear Accumulator Channel #4 High/INT #4
$3A_{16}$	R	Read & Clear Accumulator Channel #5 Low/INT #5
$3C_{16}$	R	Read & Clear Accumulator Channel #5 High/INT #5
$3E_{16}$	R	Read & Clear Accumulator Channel #6 Low/INT #6
40_{16}	R	Read & Clear Accumulator Channel #6 High/INT #6

Pulse Counter Registers

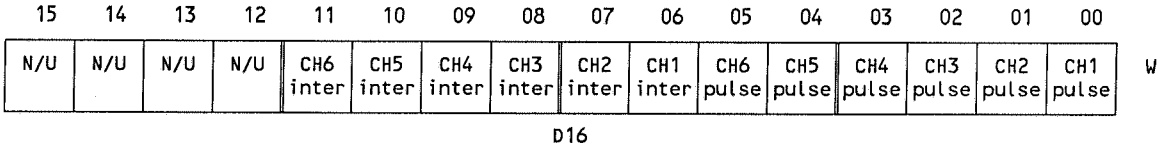


A24 OFFSET	W/R MODE	REGISTER NAME
42_{16}	W	Channel #1 Pulse Counter
46_{16}	W	Channel #2 Pulse Counter
$4A_{16}$	W	Channel #3 Pulse Counter
$4E_{16}$	W	Channel #4 Pulse Counter
52_{16}	W	Channel #5 Pulse Counter
56_{16}	W	Channel #6 Pulse Counter

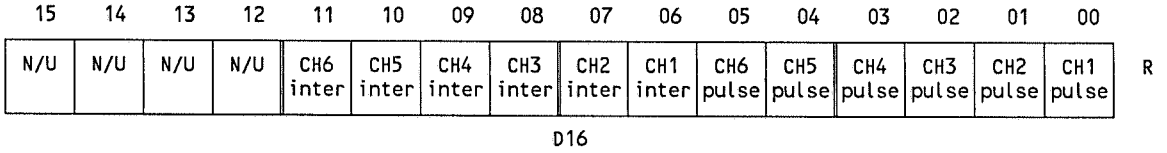
Interval Timer/Clear Accumulators Register $5A_{16}$



Interrupt Mask Register $5E_{16}$



Interrupt Status Register 62_{16}



Interrupt Status Register 66_{16}