*****Special Option*****

Model V630-S001

4-channel 50 KHz Frequency Counter

March, 1995

Special Option

Model V630-S001

The Model V630-S001 is the same as the V630-ZA11 except it has been modified to accept an input range from 20 millivolts to 10 volts. A +/-10 millivolt hysteresis is built in for the 20 millivolts to 1 volt range. For the 1 volt to 10 volt range, the hysteresis is +/-20 millivolts.

*****Special Option*****

Model V630-S002

4-channel, 50 kHz Frequency Counter

October, 1996

*****Special Option*****

Model V630-S002

The Model V630-S002 is the same as the V630-LB11 except it has been modified to accept an input range from 20 millivolts to 20 volts.

October 24, 1996

Model V630-LA/B11

4-Channel 50 KHz Frequency Counter

INSTRUCTION MANUAL

March, 1998

CONTENTS

FIGURES

TABLES

4-channel, 50 kHz Frequency Counter

Counts from 0.06 Hz to 50 kHz without changing ranges

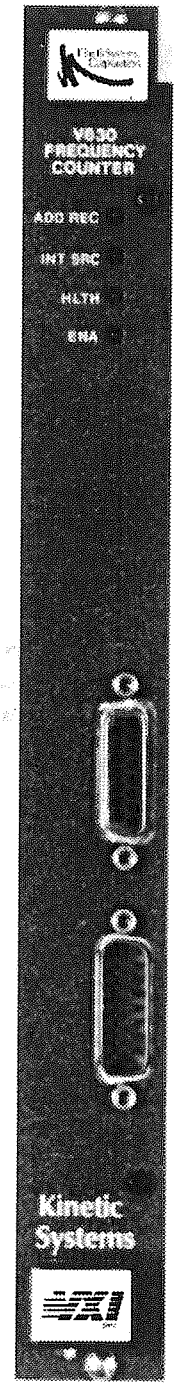
V630

Features

- **Four frequency counter channels**
- **Frequency range from 0.06 Hz to 50 kHz**
- **Options for input ranges of 100 mV to 10 V (p-p) and 1 V to 20 V (p-p)**
- **Differential inputs for high noise immunity**
- **Programmable observation window from 1 ms to 1.024 s**
- **Precision time base (±1 ppm, 10°C to 50°C)**

Typical Applications

- **Monitoring shaft encoders and other devices to measure RPM from shafts on automotive and jet aircraft engines**
- **General-purpose monitoring of input pulses**



General Description

The V630 is a single-width, C-size, register-based, VXIbus module that provides four frequency measurement channels. This counter module can be used to monitor a variety of pulse sources. Moreover, its unique circuitry allows the monitoring of a wide range of frequencies without changing any module settings. For example, the RPM of an aircraft engine shaft can be monitored at full speed as well as when it is coasting to a stop. Differential input circuits with filtering and hysteresis are used to provide high noise immunity.

Frequency measurement is armed by software command or by the receipt of an external signal, and begins when the first "edge" of the input signal is received. The input pulse stream for each channel is sampled during a user-selected observation window. The window period is programmable or can be supplied through a front-panel connector, and the selection is common to all four channels. At the end of each window period, 24 bits of data representing the timebase count from the master clock, as well as 16 bits representing the number of whole periods observed are stored in the Current Value Table (CVT) for that channel. If the period of the input pulse stream is longer than the window period, the window remains "open" until one whole period of the input signal is observed. The CVT "scratchpad" memory can be read by software at any time, with the data from the latest observation being read. The frequency can be calculated by host computer software using the following formula:

Frequency = whole input periods x clock rate/timebase counts

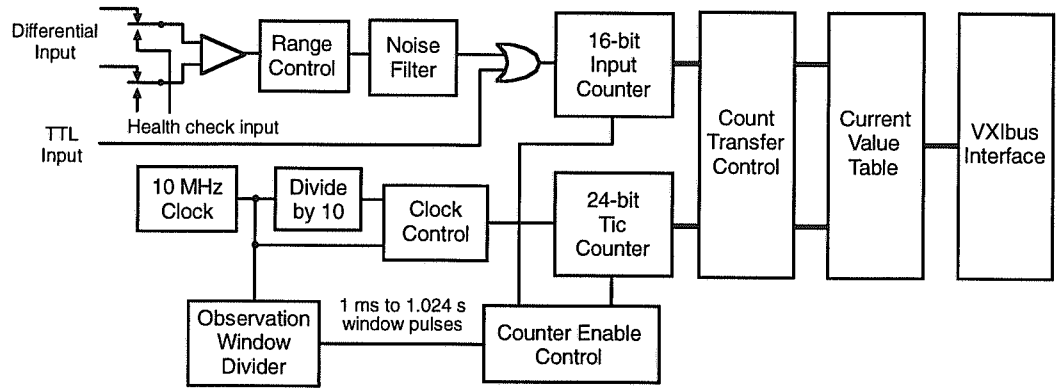
The V630 can operate in a single-scan or in a continuous mode. The clock rate for the module is programmable to provide a tick rate of 1 MHz or 10 MHz with a clock accuracy of ±0.001%. The counting accuracy depends on the time base accuracy as well as the monitoring resolution. The longer the observation window, the higher the accuracy. A 10 ms observation window will result in an accuracy of approximately ±0.01% with a 1 MHz clock, and ±0.001% with a 10 MHz clock. A 100 ms window will provide accuracies an order of magnitude better. Programming the clock to 1 MHz allows a measurement down to 0.06 Hz, while a 10 MHz clock increases the resolution by a factor of 10, but makes the lower counting limit 0.6 Hz. An overflow status bit is asserted for that channel whenever the input frequency is below the measurable limit.

A separate input connector is provided for a "health check" signal. The input circuitry can be switched—under program control—from each of the channels to this input, providing a test of the operating characteristics of that channel.

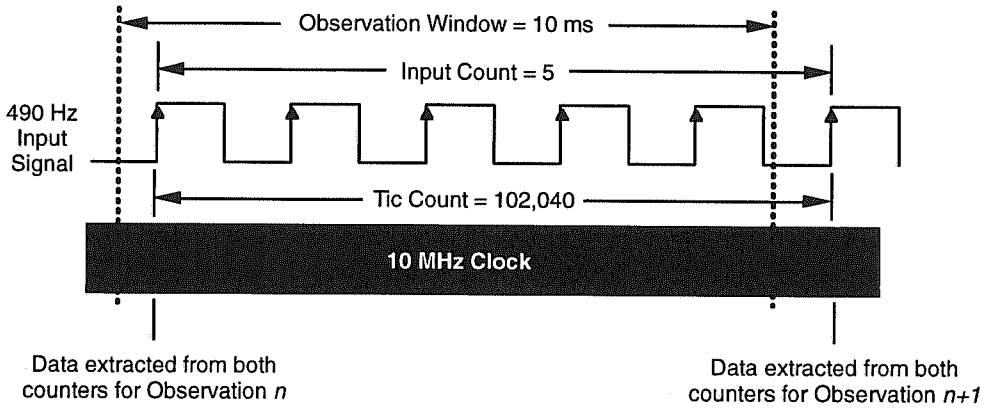
Maskable interrupt source bits are set by an overflow from the time base clock counter. An interrupt can be generated by any one or a combination of these bits.

The V630 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.

V630 Block Diagram (one channel shown)



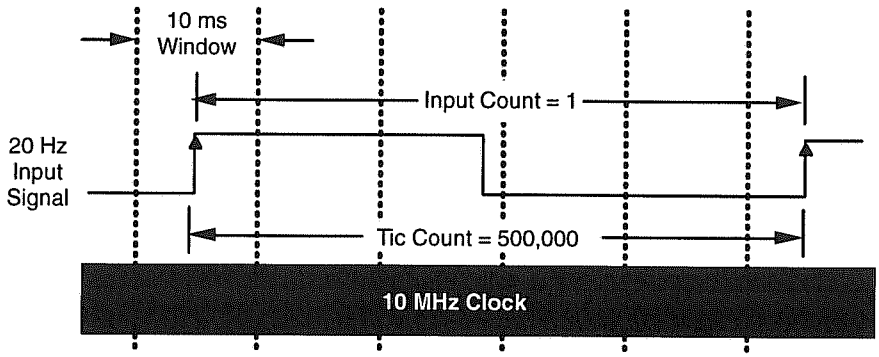
Typical Timing Sequences



Notes: 1. The frequency calculation is: 5 x 10,000,000 / 102,040 = 490.0039 Hz. The clock resolution of ±1 count could result in readings from 489.999 to 490.0087 Hz. A 100 ms window will reduce this error by a factor of 10.

2. The counting for an observation window period starts at the first input signal low-to-high transition after a window edge and stops with the first such transition after the next window edge.

3. The observation window timing is not included in the calculation. The window only controls the minimum observation time for frequencies whose period is equal to or less than one window time.



Notes: 1. The frequency calculation is: 1 x 10,000,000 / 500,000 = 20.00000 Hz with a ±0.00004 Hz resolution "jitter."

2. For a 10 ms observation window, any input signal whose period is greater than 10 ms (a frequency less than 100 Hz) will result in an input count of 1. The tic count will not terminate until one whole input period is counted or the tic counter for that channel overflows (after a count of 16,777,215).

3. The previous count will be in the current value table until another whole period is measured.

Item	Specification
Inputs	
Number of input channels	4
Input signal range	
-LA11	100 mV to 10 V, p-p
-LB11	1 V to 20 V, p-p
Input protection	Inputs are diode clamped to ±10 V
Common-mode input voltage	±10 V
Common-mode rejection	-90 dB @ 10 kHz
Input impedance	1 MΩ
Drift	2 µV/°C
Input frequency range	0.06 Hz to 50 kHz
Filtering	
Filter type	Single-pole, low-pass RC type
-3 dB cutoff frequency (f_c)	50 kHz
Hysteresis	300 mV
Time Base	
Clock rate	1 MHz to 10 MHz, programmable
Stability	±1 ppm, +10°C to +50°C
Observation Window	From 1 ms to 1.024 s, in 1 ms increments
Counter Sizes	
Time base counter	16,777,215 (24 bits)
Input pulse counter	65,535 (16 bits)
Input Connector Types	
Input signal connector	15S "D"
Calibration/diagnostic connector	15P "D"
Mating Connectors	
Input signal connector	KineticSystems Model 5936-Z1B
Calibration/diagnostic connector	KineticSystems Model 5936-Z1A
Power Requirements	
+5 V	3.9 A, typical
+24 V	150 mA, typical
-24 V	150 mA, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-sized VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V630-LA11 4-channel, 50 kHz Frequency Counter, 100 mV to 10 V input
Model V630-LB11 4-channel, 50 kHz Frequency Counter, 1 V to 20 V input

Related Products

Model 5936-Z1A Connector—15S "D" Model 5936-Z1B Connector—15P "D"

UNPACKING AND INSTALLATION

The Model V630 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and set the various option switches to conform to the desired operating environment.

SWITCH SELECTIONS

Device Address Selection

The address switches on the V630 only affect the Configuration Registers in the short I/O address space, and respond to Address Modifier Codes 29_{16} and $2D_{16}$. The Logical Address switches LA128 to LA1 determine the base address of the V630 Configuration Registers. The default setting is 255 ($FFC0_{16}$) which enables dynamic configuration of the V630. Changing the default setting disables dynamic mode and enables static configuration.

WHEN SELECTING A BASE ADDRESS, CARE SHOULD BE TAKEN TO AVOID ADDRESSES ASSIGNED TO OTHER DEVICES IN THE SHORT I/O ADDRESS SPACE.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to one (VXI defined).
Bits 13 through 6 are user-selectable via the address switches LA128-LA1.
Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.
Refer to Figure 1 (page 4) for switch locations and strap settings.

Interrupt Request Selection

The V630 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 (page 4) for the switch locations and switch settings. Both banks of eight-position switches must be set to the same positions. As shown in Figure 1 (page 4) IRQ 7 is set in both banks.

The default interrupt request level for the V630 is level 7.

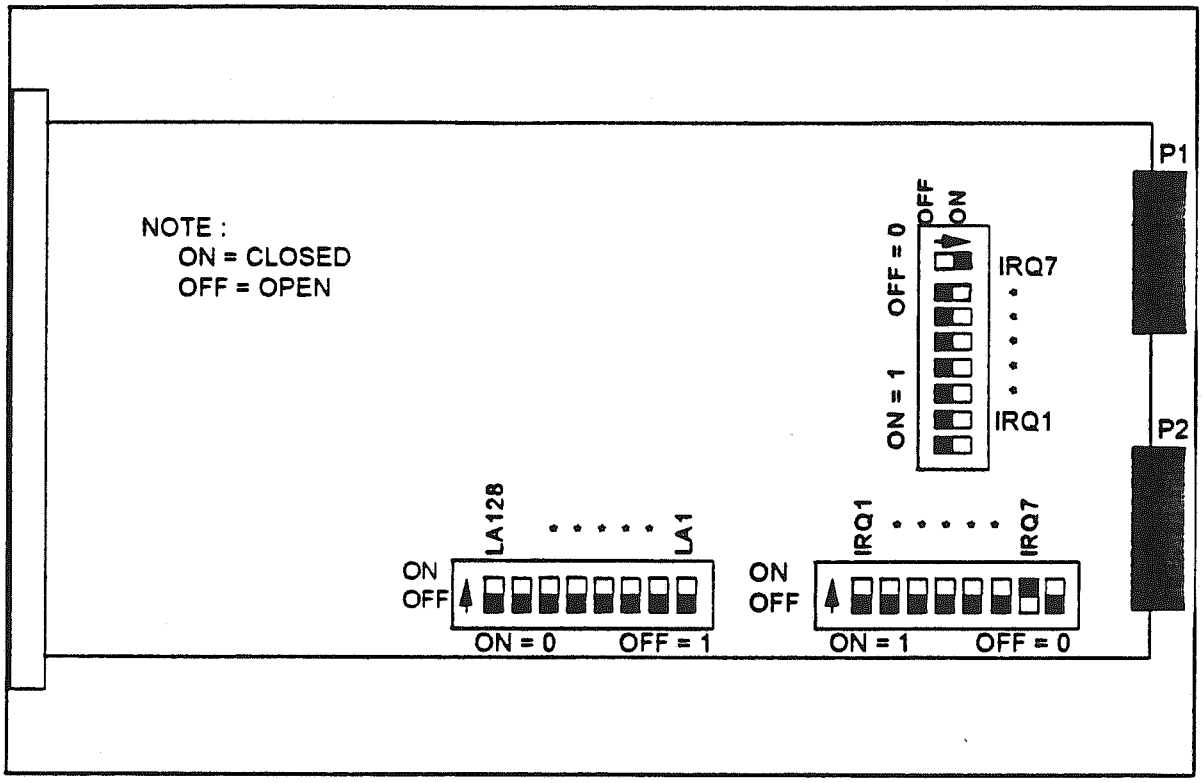


FIGURE 1 - V630 SWITCH LOCATIONS

Insertion of Module into VXIbus Mainframe

The V630 is a VXI "C" size module that requires both P1 and P2 VXI backplane connectors. The V630 can reside in any empty VXI slot except slot 0. The selected VXI slot that the V630 will reside in requires the Bus Request (BR) and Interrupt Acknowledge (IACK) straps be removed for proper VXIbus operation. Any empty slots in the VXI crate should have their BR and IACK straps loaded.

CAUTION:	**TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE**

WARNING:	**REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE IN THE BACKPLANE**

CONNECTORS

The two mounted front panel connectors provide the mechanism for connecting the V630 to the input channels. The 15 position connector, J1, contains the input signals for the four channels. Each channel input has a +, -, and shield connection. The second connector, J2, contains TTL input and output signals, as well as the +, -, and shield connections for the Health signal.

The J2 connector also contains 6 TTL input signals. The External Start signal is used to enable the V630 for scanning. The External Start signal must be a low-going TTL pulse with a minimum pulse width of 200 nanoseconds. This signal provides the same functionality as Operational register $3E_{16}$ (See Page 14). The second TTL input, Window Clock, is reserved for factory use.

The J2 connector also contains 5 TTL level output signals. Four of the signals are the conditioned input channels. These signals are labeled Conditioned 1 through 4 in the table below. The last output is the window clock output and is reserved for factory use.

The following chart shows the pinouts for the J1 and J2 connectors.

J1 AND J2 CONNECTOR PINOUTS

CONNECTOR J1 (15 position Female)			
Pin 1	Channel 1 +	Pin 9	Channel 3 +
Pin 2	Channel 1 -	Pin 10	Channel 3 -
Pin 3	Channel 1 Shield	Pin 11	Channel 3 Shield
Pin 4	Ground	Pin 12	Ground
Pin 5	Channel 2 -	Pin 13	Channel 4 +
Pin 6	Channel 2 +	Pin 14	Channel 4 -
Pin 7	Channel 2 Shield	Pin 15	Channel 4 Shield
Pin 8	Ground		

CONNECTOR J2 (15 position Male)			
Pin 1	Health Input +	Pin 9	Conditioned 3
Pin 2	Health Input -	Pin 10	CH4 TTL IN
Pin 3	Health Input Shield	Pin 11	Conditioned IN 4
Pin 4	CH1 TTL IN	Pin 12	START
Pin 5	Conditioned 1	Pin 13	GROUND
Pin 6	CH2 TTL IN	Pin 14	Window Clock Out (Reserved)
Pin 7	Conditioned 2	Pin 15	Window CLK (Reserved)
Pin 8	CH3 TTL IN		

VXI Addressing

The V630 Configuration Registers reside in the short I/O address space of the VXIbus and responds to both Address Modifier Codes 29_{16} and $2D_{16}$. The switches LA128 through LA1 determine the base address of the V630 Configuration Registers. The default base address setting is 255 which enables dynamic configuration of the V630. The default Interrupt Request level is set to Level #7. If the Base Address or the Interrupt Level need to be changed, refer to the section on Switch Selections (page 3).

In dynamic configuration, the Base Address for the Configuration Register must be changed. This is done by writing to the ID/Logical Address Register with a value other than 00_{16} or FF_{16}. The formula for a new Base Address is given below:

$$VXIbus\_Address = (64 \times Logical\_Address) + 49152$$

where (Logical_Address) is in the range of 1 to 254. The new VXIbus_Address will be in the range of $C040_{16}$ to $FF80_{16}$. Before writing the new Logical_Address, the MODID line must be set to the slot location that the V630 resides in. The Slot 0 controller is used to select or deselect MODID lines. The ID/Logical Address can now be written with the new Logical Address value. The Slot 0 controller should deselect the MODID line at this time.

The V630 Operational Registers reside in the Standard Address space of the VXIbus and respond to four Address Modifier Codes; 39_{16}, $3A_{16}$, $3D_{16}$ and $3E_{16}$. To configure and gain access to the Operational Registers, refer to the section on Operational Registers (page 9).

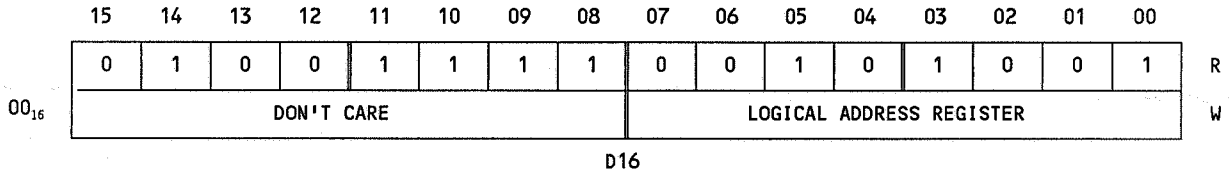
VXI CONFIGURATION REGISTERS

The following six registers occupy the short I/O (A16) address space and conform to the VXI specifications for Configuration Registers. These registers are normally used once, to configure the V630 at power-up. The Operational Registers are used the remainder of the time.

TABLE 1
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET	W/R MODE	REGISTER NAME
00_{16}	W/R	ID/Logical Address Register
02_{16}	R	Device Type Register
04_{16}	W/R	Status/Control Register
06_{16}	W/R	Offset Register
08_{16}	R	Attribute Register
$1E_{16}$	R	Subclass Register

ID/Logical Address Register (OFFSET 00_{16})

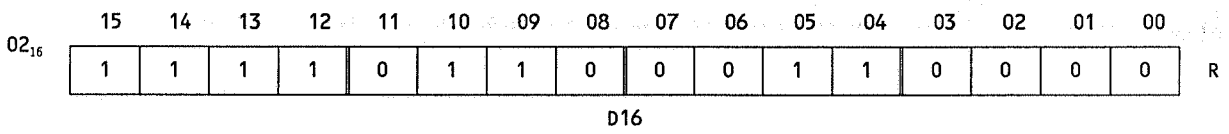


On READ transactions:

Bit(s)	Mnemonic	Meaning
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V630. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

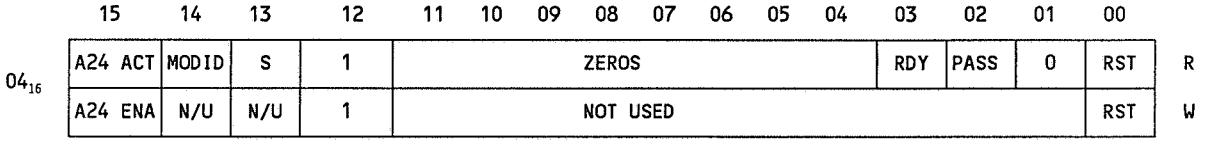
Device Type (OFFSET 02_{16})



On READ transactions:

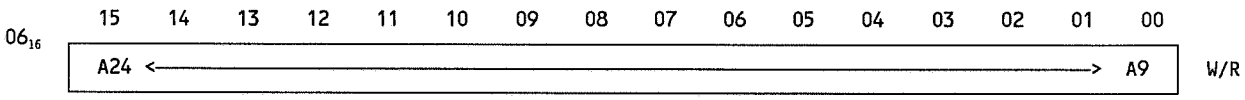
Bit(s)	Mnemonic	Meaning
15 - 12	Required Memory	The V630 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model V630 (630_{16}).

Status/Control Register (OFFSET 04_{16})



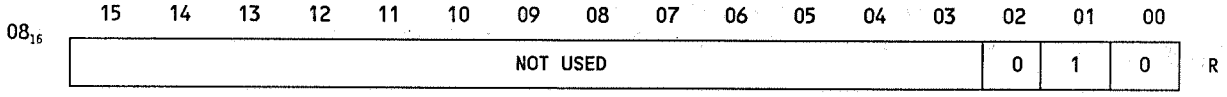
Bit	Mnemonics	Description
15	A24	Writing a "1" will enable A24 addressing and allow access to the Operational Registers. Reading a "1" indicates A24 is active. This bit is reset to a "0" on power-up or with the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on VXIbus connector P2. A "0" will indicate that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V630. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1".
11-4	N/U	Not used. Read as a zero.
3	RDY	READY. The V630 is always ready. Read as a one.
2	PASS	PASS. The V630 will always pass self tests. Read as a one.
1	N/U	NOT USED. Read as a zero.
0	RST	RESET. This Read/Write bit controls the Soft Reset condition within the V630. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Registers (see below), except the Diagnostic and Interrupt Status Registers is inhibited. The Operational Registers are maintained in the state they were in just prior to the Soft Reset being enabled. This bit can be reset by writing a "0", on power-up or the assertion of SYSRESET*.

Offset Register (OFFSET 06_{16})



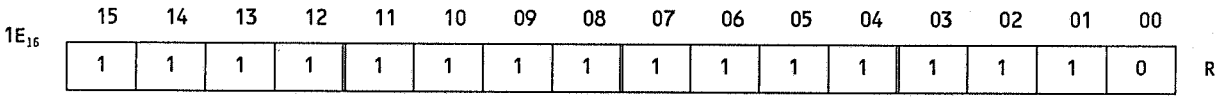
This 16-bit read/write register defines the base address for the A24 Operational Registers. This register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Attribute Register (OFFSET 08_{16})



Bit(s)	Mnemonic	Meaning
15 - 03	Not Used	These bits are not used by the V630, and are read as zeros.
02	Intr Control	The V630 has Interrupt Control capabilities.
01	Intr Handler	The V630 does not have Interrupt Handler capabilities.
00	Intr Status	The V630 has an Interrupt Status register.

Subclass Register (OFFSET $1E_{16}$)



Bit(s)	Mnemonic	Meaning
15	Extended Device	"1" indicates this to be a VXIbus defined Extended Device.
14-00	Register-Based	$7FFE_{16}$ indicates this to be an Extended register-based Device.

OPERATIONAL REGISTERS

To gain access to these registers, write to the Configuration Offset Register to set the A24 base address. Then write to the Configuration Status/Control Register with Bit 15 set to a "1". The Operational Registers are enabled and set to the desired based address. Any access to the Operational Register must be word (D16) transfer. A description of the Operational Registers is described below:

TABLE 2
V630 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

A24 OFFSET	W/R MODE	REGISTER NAME
00_{16}	W/R	Diagnostic Register
02_{16}	R	Interrupt Status Register
12_{16}	W	Current Value Table Address
16_{16}	R	Current Value Table Data
18_{16}	R	CVT Tic Count High
$1A_{16}$	W	Control Register
$1E_{16}$	R	Control Register
22_{16}	R	Overflow INT Status Register
26_{16}	R	Overflow INT Request Register
$2A_{16}$	W	Overflow INT Mask Register
$2E_{16}$	W	Selectively Clear Overflow INT Status Bits
32_{16}	R	Stop Scanning
36_{16}	R	Single Scan
$3A_{16}$	R	Clear Current Value Table Address Register
$3E_{16}$	R	Enable Continuous Scanning
42_{16}	R	Disable Continuous Scanning
46_{16}	R	Enable Overflow INT Request
$4A_{16}$	R	Disable Overflow INT Request
$4E_{16}$	R	Clear Overflow INT Status Bits
56_{16}	R	Test for Overflow Status
$5A_{16}$	R	Test for Scanning Active

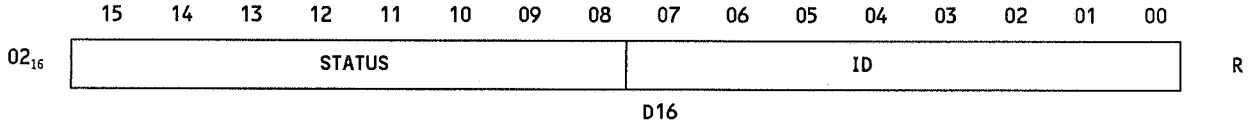
Diagnostic Register 00 (OFFSET 00_{16})

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care.								D	S	0	INT ENA	INT SRC	0	0	0	R
00_{16}	Don't Care.								0	0	0	INT ENA	0	0	0	INIT	W
	D16																

Bit	Mnemonic	Description
15-8	D/C	Don't Care.

7	Diagnostic	When this bit is set to a "1", the last register access to the Operational Registers (12_{16} through $5A_{16}$) is valid.
6	Status	When this bit is set to a "1", the last register access to the Operational Registers (12_{16} through $5A_{16}$) is accepted.
5	N/U	Not Used.
4	INT ENA	Interrupt Enable: Setting this bit to a "1" will enable interrupts.
3	INT SRC	Interrupt Source: When this bit is set to a "1", the "TIC" Counter on the V630 has overflowed. (See Page 19.)
2, 1	N/U	Not Used.
0	INIT	Setting this bit to a "1" will initialize the Operational Registers (12_{16} through $5A_{16}$). The Configuration Registers and the Diagnostic Register are unaffected.

Interrupt Status/ID Register (OFFSET 02_{16})



This is a Read-Only 16-bit Interrupt Status Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.

Bit	**Mnemonic**	**Description**
15-8	STATUS:	These eight bits will indicate Request True or Request False. Request True = FD_{16} Request False = FC_{16}
7-0	ID:	These eight bits represent the Logical Address of the V630 Configuration Registers.

Current Value Table (CVT) Address (OFFSET 12_{16})

This register is used to write the CVT Address. After this command is executed, the CVT Address Register points to the requested entry in the CVT. Legal write data values for this command are 0 through 8. The Status bit in the Diagnostic Register will always equal a one.

Current Value Table (CVT) Data (OFFSET 16_{16})

This register is used to read the data contained in the Current Value Table (CVT). After the data at the addressed location has been read, the CVT address register is incremented.

The first entry in the Current Value Table contains the Status Word. Refer to the Current Value Table section (page 16) of this manual for further information on the Status Word. The next eight entries in the CVT contain the Period Count and Tic Count values for each of the four channels. Refer to the Current Value Table section (page 16) of this manual for a detailed description of the CVT. After the Tic Count data for channel 4 has been read, the Current Value Table Address Register is automatically reset to zero, thus pointing to the Status Word.

Tic Count High Data (OFFSET 18_{16})

The second half of the Tic Count from the Current Value Table Register is read from this register. When the Tic Count is read from the CVT, this register must be read to obtain the full 24-bit Tic Count Word. The CVT address must be at address 2, 4, 6 or 8 when a read from the CVT data register is executed. Once this is done, a read from Tic Count High Data Register must be executed.

Write Control Register (OFFSET $1A_{16}$)

This register is used to write data into the Control Register. This register may only be written while input scanning is disabled. If this command is executed while scanning is enabled, the command is ignored and the status bit in the Diagnostic Register will equal a "0". The status bit will equal a "1" if the register access, when scanning, is disabled. This register is reset to "0" on power-up and after a SYSRESET*. Refer to the Control Register section of this manual on Page 14 for further information.

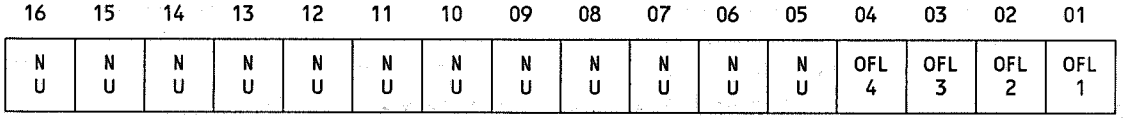
Read Control Register (OFFSET $1E_{16}$)

This register is used to read the contents of the Control Register. Refer to the Control Register section of this manual for further information. The Status bit in the Diagnostic Register will always equal a one.

Overflow Interrupt Status (OFFSET 22_{16})

The Interrupt Status Register is a 16-bit read-only register which provides access to the four channel overflow Interrupt Status bits. The Interrupt Status bits may also be read in the Current Value Table Status Word location. Refer to the Current Value Table section (page 16) of this manual for additional information. A bit read back as a "1" indicates that the corresponding channel has overflowed. These bits are cleared on power-up, the assertion of

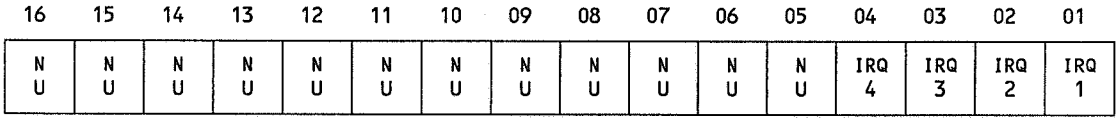
the assertion of the SYSRESET* signal, a Clear Interrupt Status command, and a Selective Clear Interrupt Status command. The following diagram shows the bit layout for the Interrupt Status Register.



Bit	Mnemonic	Description
16:05	NU	NOT USED. These bits are not used and are read as "0".
04:01	OFL4-OFL1	OVERFLOW 4 THROUGH 1. These bits represent the overflow bits for the individual channels.

Overflow Interrupt Request (OFFSET 26_{16})

The Interrupt Request Register is used to determine the source of an Interrupt generated by the V630. An Interrupt is asserted when Interrupt Requests are enabled AND an Interrupt Status bit is true AND its corresponding Interrupt Mask bit is enabled (set to a "1"). The Interrupt Request Register is a read-only register and is cleared on power-up, a SYSRESET* signal, a read from register $4E_{16}$ (Clear Interrupt Status), or a selective clear operation to the individual Interrupt Status bits. The following diagram shows the bit layout for the Interrupt Request Register.



Bit	Mnemonic	Description
16:05	NU	NOT USED. These bits are not used and are read as "0".
04:01	IRQ4:IRQ3	INTERRUPT REQUEST 4 THROUGH 1. These read-only bits indicate which channel overflow is generating a Interrupt Request. If IRQ3 is read as a "1", it indicates that channel 3 has overflowed AND its corresponding Interrupt Mask Register bit is set to a "1".

Overflow Interrupt Mask (OFFSET $2A_{16}$)

The Interrupt Mask Register is used to specify which of the four Interrupt sources are to generate an Interrupt Request. If an Interrupt Source is to assert a VXI Interrupt, it must first be masked in the Interrupt Mask Register. A Interrupt Source is masked on by writing

the corresponding Interrupt Mask bit to a "1". An Interrupt Mask Register is written to $2A_{16}$. Each bit position in the Interrupt Mask Register corresponds to the same Interrupt Status bit in the Interrupt Status Register. The Interrupt Mask Register is reset to "0" on power-up, a SYSRESET* signal, or setting bit "1" in the diagnostic Register. The following diagram shows the bit layout for the Interrupt Mask Register.

16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	MSK 4	MSK 3	MSK 2	MSK 1

Bit	Mnemonic	Description
16:05	NU	NOT USED. These bits are not used and should be written as "0".
04:01	MSK4:MSK1	MASK 04 THROUGH MASK 01. These write-only bits are used to enable/disable the generation of an Interrupt Request by the corresponding Interrupt Status bits.

Selectively Clear Interrupt Status (OFFSET $2E_{16}$)

This register clear operation does not affect the Interrupt Mask Register bits or the Interrupt Request enable. Register $2E_{16}$ is used to selectively clear the Interrupt Status bits. For this register, the data is set equal to the Interrupt Status bits that are to be cleared. For example, to clear Interrupt Status bit 3, the write data would be set to 4. To clear both Interrupt Status bits 1 and 2, the write data would be set to 3. The Status bit in the Diagnostic Register will always equal a "1".

OPERATIONAL CONTROL REGISTERS

The V630 has ten Operational Control Registers at offset 32_{16} through $5A_{16}$. These registers are Read-Only and return a 16-bit data code. There are only two possible codes that can be returned. The first data code will return a value of "0" and has the same meaning as the Status bit in the Diagnostic Register set to Logical "0". The second data code will return a value of "1" and has the same meaning as the Status bit in the Diagnostic Register set to a Logical "1". This data code will indicate the command was accepted or a test condition is true when equal to "1". These ten Operational Control Registers are described below:

Stop Scanning (OFFSET 32_{16})

This register is used to stop the V630 from scanning its inputs, and reset the CVT Address Register. A data code of "1" is returned only when scanning is enabled. If this register is read while scanning is disabled, a data code of "0" is returned. After this command is executed, the V630 must be re-enabled if scanning is to resume.

Single Scan (OFFSET 36_{16})

This register is read to initiate a single scan of the input channels. This register returns a data code of "1" as long as the V630 is not scanning. If this register is read while the V630 is in the process of scanning, a data code of "0" is returned.

Clear Current Value Table Address (OFFSET $3A_{16}$)

This register is read to reset the CVT Address Register to "0". A data code of "1" is always returned for this register.

Enable Continuous Scanning (OFFSET $3E_{16}$)

This register is read to enable the V630 for input scanning. A data code of "1" is always returned for this register. Once scanning is enabled, the V630 starts converting the input channel data into frequency measurements.

Disable Continuous Scanning (OFFSET 42_{16})

This register is read to disable the V630 from scanning the input channels. A data code of "1" is always returned for this register. Scanning is disabled on power-up, the assertion of the SYSRESET* signal, or setting bit one in the Diagnostic Register.

Enable Overflow INT Request (OFFSET 46_{16})

This register is read to enable the generation of a Interrupt Request upon the occurrence of a Interrupt Source. A data value of "1" is always returned for this register. A Interrupt Request is generated if a Interrupt Source is pending AND the corresponding Interrupt Mask bit is set to a one AND the Interrupt Request is enabled. The Interrupt Request is disabled on power-up, the assertion of the SYSRESET* signal, or setting bit one in the Diagnostic Register.

Disable Overflow INT Request (OFFSET $4A_{16}$)

This register is read to disable all Interrupt Requests. A data code of "1" is always returned for this register. The Interrupt Requests are always disabled on power-up, the assertion of the SYSRESET* signal, or setting bit one in the Diagnostic Register.

Clear Overflow Status (OFFSET $4E_{16}$)

This register is read to clear all four of the Interrupt Status bits. A data code of "1" is always returned for this register. If it is necessary to clear the Interrupt Status bits individually, the Selective Clear Interrupt Status Bit command may be used. Refer to the Selectively Clear Interrupt Status section of this manual for further information.

Test Overflow Status (OFFSET 56_{16})

This register is read to test for the presence of an Interrupt Source. If an Interrupt Source is pending when this register is read, a data code of "1" is returned. A data code of "0" is returned when this register is read and an Interrupt Source is not pending.

Test Scan Active (OFFSET $5A_{16}$)

This register is read to test for scanning activity within the V630. If this register is read while the V630 is scanning, a data code of "0" is returned. If the V630 is not scanning and this register is read, a data value of "1" is returned.

CURRENT VALUE TABLE

The Current Value Table (CVT) is composed of the Current Value Table Status Word (CVTSW) and eight information words, two for each channel. The two entries for each channel include the Period Count and the Tic Count. These two entries are used for the calculation of the input frequency. The following diagram shows the locations of the status word and the four channel Period Count and Tic Count.

ADDRESS	CURRENT VALUE TABLE DATA
0	STATUS WORD
1	CHANNEL 1 PERIOD COUNT
2	CHANNEL 1 TIC COUNT
3	CHANNEL 2 PERIOD COUNT
4	CHANNEL 2 TIC COUNT
5	CHANNEL 3 PERIOD COUNT
6	CHANNEL 3 TIC COUNT
7	CHANNEL 4 PERIOD COUNT
8	CHANNEL 4 TIC COUNT

The frequency of the input signal can be determined from the contents of the Current Value Table and the selected time base clock rate. The formula is:

Frequency = whole number of input periods X clock rate/Tic counts

The Current Value Table (CVT) is read through register 16_{16}. The data word returned for this command is dependent on the Current Value Table Address Register (CVTAR). This register points to the CVT entry that is to be accessed. After a read from CVT data register 16_{16}, the CVT Address Register is automatically incremented and points to the next sequential location in the CVT. After all elements in the CVT have been read (i.e., the address register is 8), the CVT Address Register is automatically reset to zero.

The CVT Address Register can be written by writing to register 12_{16} with data equal to the CVT address to be read. Legal write data values are from 0 to 8. A read from register $3A_{16}$ will reset the CVT Address Register to zero.

Circuitry on the V630 prevents a channel entry in the CVT from being updated while the data is being read. For example, if the channel 3 Period Count word has been read from the CVT, but the Tic Count word has not been read, the CVT is not updated until channel 3 Tic Count word has been read. This is done to prevent erroneous data readouts from the CVT.

The first entry in the CVT is the Current Value Table Status Word (CVTSW). This word contains two bits which define the current operating parameters of the V630. There are also two bits for each channel which reflect the channels status.

Bit 16 of this word indicates the current operating mode of the V630. If this bit is read as a "1", it indicates that all channels of the V630 are scanning the Health signal input. If this bit is a "0", each channel of the V630 is scanning its individual channel input.

Bit 15 of the CVTSW reflects the Tic rate of the V630. If the bit is read as a "1", the Tic rate is 1 Megahertz (1 microsecond cycle). A "0" for this bit indicates that the 10 Megahertz (100 nanosecond cycle) Tic rate is in use. The 10 Megahertz rate can measure frequencies greater than .59 Hz, while the 1 Megahertz rate can measure frequencies greater than .059 Hz.

Bit 9 of the CVTSW is set whenever either of bits 8 through 5 are set in the CVTSW. This bit may be tested by software to determine if any overflow condition has occurred.

Bits 8 through 5 are set whenever an individual channel overflow condition occurs. An overflow condition occurs when the Tic Counter exceeds a count of 16,777,215 (FFFFFF Hex). (.59 Hz for 10 MHz Clock Rate) This overflow condition indicates that the Tic rate should be reduced.

Bits 4 through 1 are set to a "1" when a particular channels' data is stale. Stale data refers to CVT data that has been read once and has not been updated in the CVT since the last read operation. After channel data has been updated in the CVT, the corresponding Stale data bit is reset to "0". The following diagram shows the bit layout of the Current Value Table Status Word (CVTSW).

16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
HLTH ENA	CLK SEL	N U	N U	N U	N U	N U	GBL OFL	OFL 4	OFL 3	OFL 2	OFL 1	STL 4	STL 3	STL 2	STL 1

Bit	Mnemonic	Description
16	HLTH ENA	HEALTH ENABLE. This bit is read as a "1" when the Health signal input is being scanned by all channels. If this bit is read as a "0", the V630 is scanning the individual channel inputs.
15	CLK SEL	CLOCK SELECT. This bit is read as a "1" when the selected Tic rate is 1 Megahertz. A "0" is returned for this bit if the Tic rate is 10 Megahertz.

14:10	NU	NOT USED. These bits are not used and are read as zeros.
09	GBL OFL	GLOBAL OVERFLOW. This bit is returned set to a "1", whenever any of bits 8 through 5 are set in the CVTSW.
08:05	OFL4:OFL1	OVERFLOW 4 THROUGH 1. These bits are set to a "1" whenever an individual channel overflow condition occurs.
04:01	STL4:STL1	STALE DATA 4 THROUGH 1. These bits are set to a "1" when an individual channels' data has been read and are then reset to "0" when a subsequent CVT update occurs for that channel.

CONTROL REGISTER LAYOUT

The Control Register is used to define the operation parameters of the V630. Selections in this register include the sampling clock tic rate, a health check enable, and the sampling window interval. This register is loaded by writing to register $1A_{16}$ and may only be written when the V630 is not enabled for scanning. The Control Register may be read by reading register $1E_{16}$. The following diagram shows the bit layout of the Control Register followed by a description of the bits.

16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
HLTH ENA	CLK SEL	N U	N U	N U	N U	WSEL 10	WSEL 09	WSEL 08	WSEL 07	WSEL 06	WSEL 05	WSEL 04	WSEL 03	WSEL 02	WSEL 01

Bit	Mnemonic	Description
16	HLTH ENA	HEALTH ENABLE. This bit is used to enable and disable the input health signal. Setting this bit to a "1" routes the Health input to each of the four channels. When this bit is set to a "0", the four individual inputs are routed to the corresponding channels. This bit is cleared on power-up.
15	CLK SEL	CLOCK SELECT. This bit is used to select the Tic clock rate used to make the frequency measurement. Setting this bit to a "1" selects Tic clock rate of 1 Megahertz (1 microsecond cycle). A Tic clock rate of 10 Megahertz is obtained when this bit is set to "0". This bit is cleared on power-up.

14:11	NU	NOT USED. These bits are not used and are read as zeros.
10:00	WSEL10-WSEL00	WINDOW SELECT 10 THROUGH 00. These bits are used to select the sampling window size. This selection ranges from 1 millisecond to 1.024 seconds. The incremental step size for these selections is one millisecond. Valid Data Values for these bits are 0 to 1023. Note: A value of 0 indicates a 1.024 second window. A value of 1 indicates a 1 millisecond window.

INTERRUPTS

The V630 can generate an Interrupt from one of four sources. Each channel may generate an Interrupt when the Tic Counter overflows. The Tic Counter for a given channel overflows when the Tic Count for a sampling window period exceeds 16,777,215 (FFFFFF hex). This overflow condition indicates that the Tic Clock rate should be reduced.

The V630 must be setup properly in order to interrupt the VXIbus. First, the interrupt switches must select one of seven Interrupt Requests by switching the appropriate IRQ switches to the "ON" position. Refer to the Interrupt Request Switch Selection for further information. Next, enable interrupts in the following manner:

Enable the Overflow INT request by reading the ENA Overflow INT request register (OFFSET 46_{16}).

Enable Interrupts to the VXIbus by writing Bit 4 in the Diagnostic Register (OFFSET 00_{16}) with a Logical "1".

The V630 is now able to cause an interrupt on the VXIbus. Once the V630 sets an interrupt, an interrupt handler will read the Status/ID Register and reset the Enable Interrupt bit in the Diagnostic Register to a Logical "0". At this time, the interrupt request should be cleared which will also clear INT SRC in the Diagnostic Registers to a Logical "0". To clear an Interrupt request, register $2E_{16}$ or $4E_{16}$ may be used to clear Interrupt Status bits. Once INT SRC Bit 3 in the Diagnostic Register is set to a Logical "0", the Interrupt Enable Bit 4 in the Diagnostic Register can be set to a Logical "1". If INT SRC is a Logical "1" when INT ENA is set to a Logical "1", an interrupt will occur instantly.

FRONT PANEL

LEDs

ADD_REC	This LED turns on only when an Operational Register (OFFSET 12_{16} through OFFSET $5A_{16}$) is accessed. The Operational

Registers must be enabled by setting bit #15 in the Status/Control Register.

INT SRC — This LED turns on when a overflow has occurred and Overflow INT request is enabled.

ENABLE — When this LED is on, the V630 is enabled for scanning.

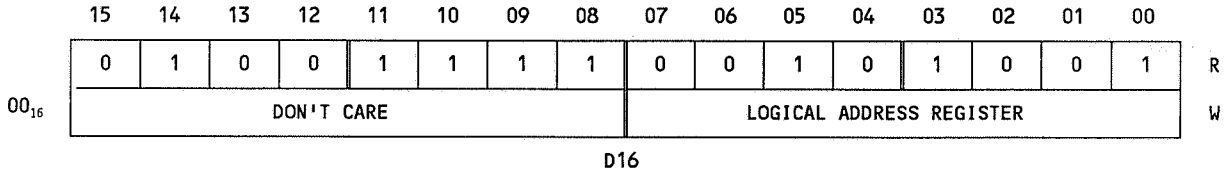
HLTH — When this LED is on, the V630 has the Health input signal enabled.

APPENDIX

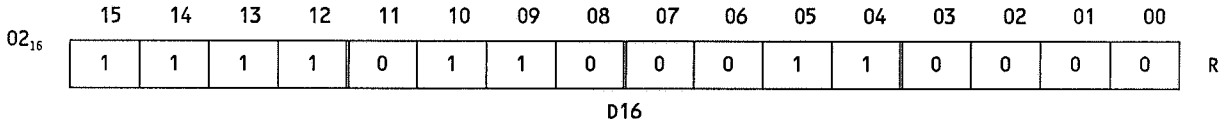
V630 REGISTER LAYOUT

CONFIGURATION REGISTERS

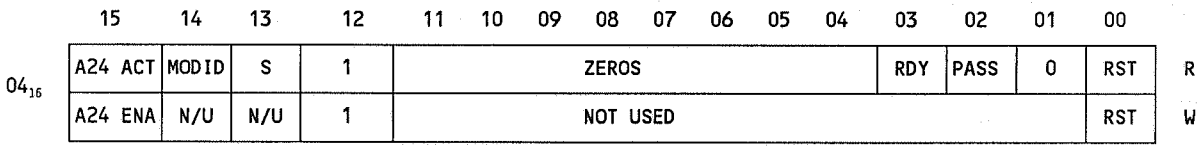
ID/Logical Address Register



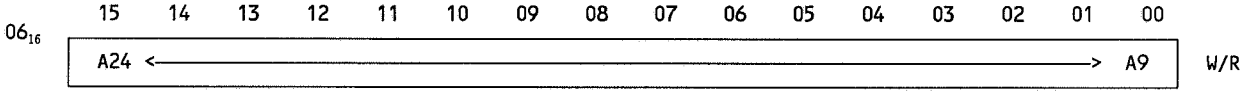
Device Type



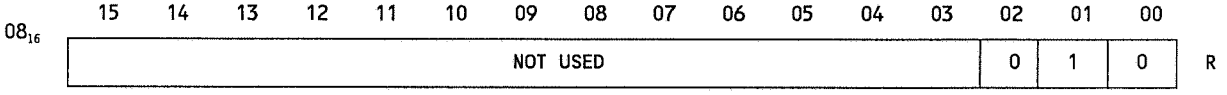
Status/Control Register



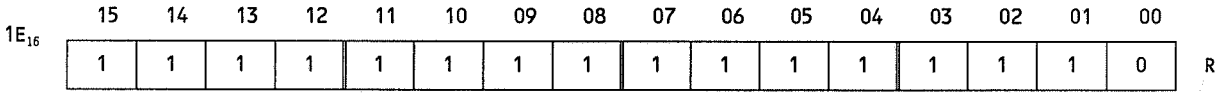
Offset Register



Attribute Register

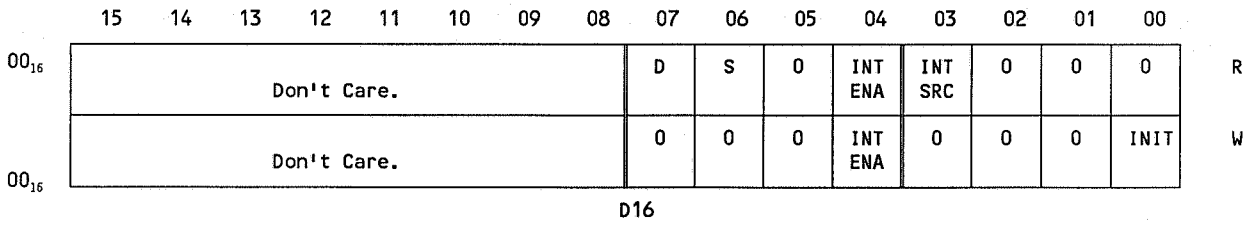


Subclass Register

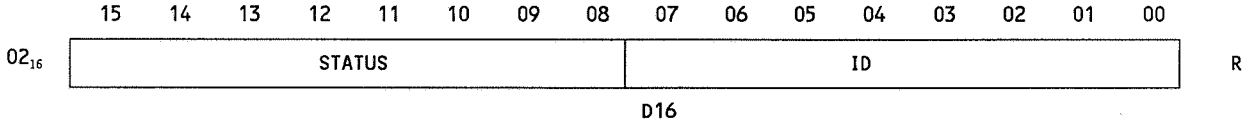


OPERATIONAL REGISTERS

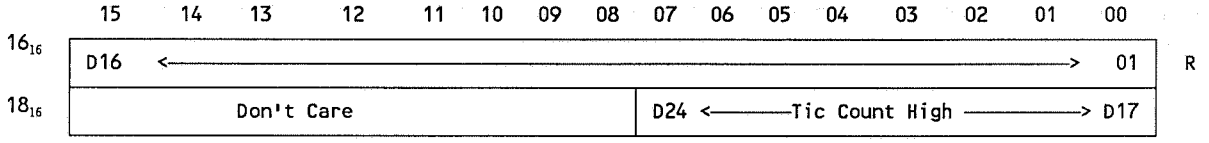
Diagnostic Register



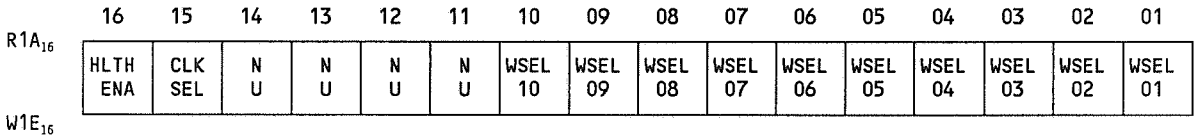
Interrupt Status/ID Register 02



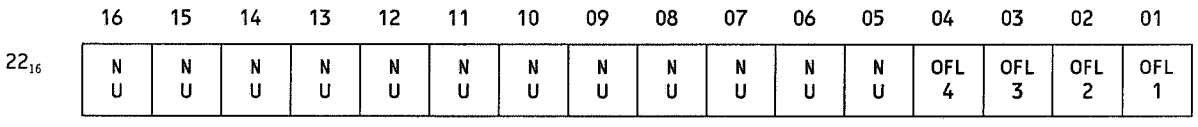
Current Value Table



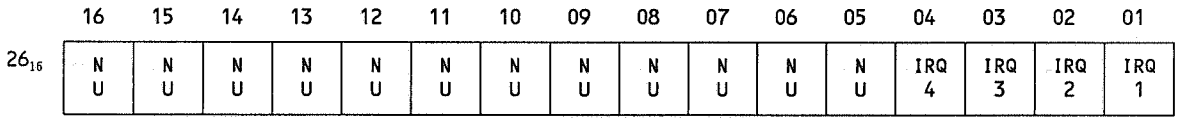
Control Register



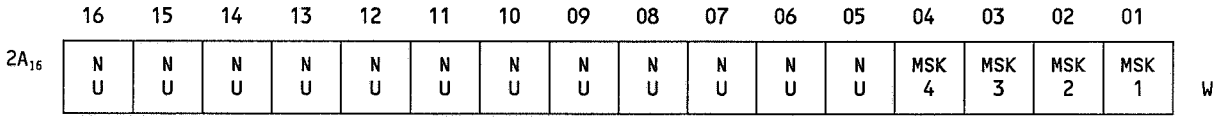
Overflow Interrupt Status



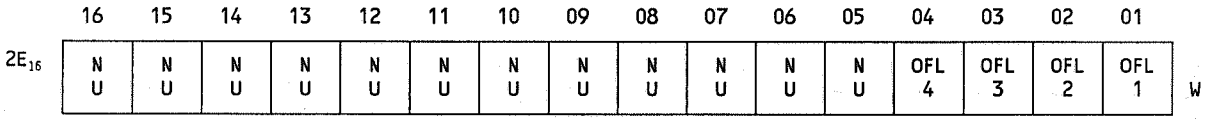
Overflow Interrupt Request



Overflow Interrupt Mask



Selectively Clear Interrupt Status



CONTROL REGISTERS

32_{16}	Stop Scanning
36_{16}	Single Scan
$3A_{16}$	Clear Current Value Table Address
$3E_{16}$	Enable Continuous Scanning
42_{16}	Disable Continuous Scanning
46_{16}	Enable Overflow INT Request
$4A_{16}$	Disable Overflow INT Request
$4E_{16}$	Clear Overflow Status
56_{16}	Test Overflow Status