Model V645-LA11/LB11

8-Channel Timing Pulse Generator

INSTRUCTION MANUAL

March, 1998

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FIGURES

TABLES

Warranty
NPD:rem(WP)

8-channel Timing Pulse Generator

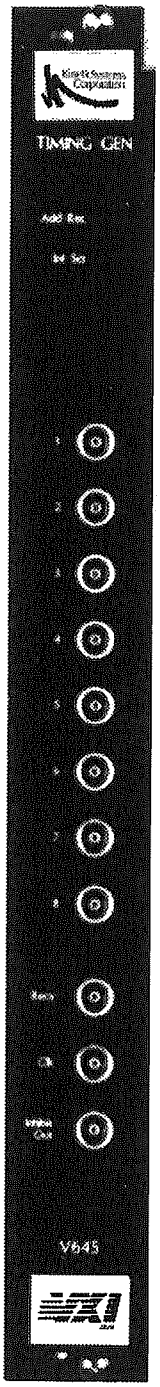
Generates an output timing sequence with up to 8 pulses **V645**

Features

- **Eight independent outputs**
- **Self-contained crystal clock**
- **Provision for external clock**
- **Options for high-true or low-true output pulses**
- **Interrupt source bits associated with each output channel**
- **8-bit interrupt mask register**
- **Clock rates from 1 Hz to 1 MHz in decade steps**
- **Ability to cycle through any number of channels from one to eight**

Typical Applications

- **Test cells**
- **Nuclear accelerator control and monitoring**
- **General-purpose time sequence generation**



General Description *(Product specifications and descriptions subject to change without notice.)*

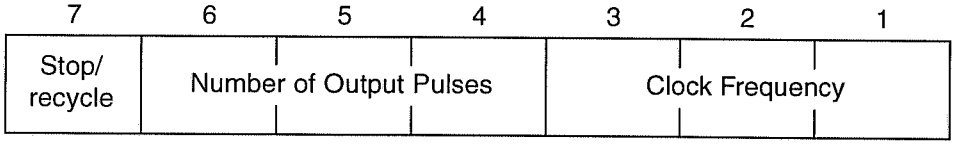
The V645 is a single-width, C-size, register-based, VXIbus module that contains a 16-bit counter and eight 16-bit set-point registers that are compared with the counter. The comparisons produce output pulses, and any of them can be used to either stop or clear the counter. The comparisons also produce interrupt source bits which can be individually enabled to produce interrupt requests.

A flag bit determines whether the counter stops with the last output pulse or whether it is cleared to produce repeated cycles of timing sequences. In the former mode of operation, additional pulse sequences are initiated either by a software command or by an external signal or contact closure.

The V645 provides its own crystal clock, and the input frequency to the counter is software-controlled for any decade from 1 Hz to 1 MHz. Input to the counter can also come from an external source.

Numbers in the eight registers (or fewer, if less than eight pulse sources are required) must be stored in increasing numerical order for proper timing of the output pulses.

A control register provides programmable control of the clock frequency (1 Hz to 1 MHz), the number of channels that generate a pulse (one to eight), and whether to stop or recycle after the last pulse. The bit assignments in the register are shown below:



Bits 1, 2, 3 = N, where clock frequency = 10N Hz (except N = 7 selects the external input.)

Bits 4, 5, 6 = P, where P + 1 = number of channels that generate a pulse.

Bit 7 = "1" to continuously cycle, "0" to cycle once and stop.

The V645 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.

Item	Specification
Number of Outputs	8
Output Pulse Width	200 ns
Clock Selection	1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz; external, TTL input
Internal Clock Source	
Overall stability	±0.01%, 0°C to +70°C
External Clock Source	
Maximum input frequency	25 MHz
Minimum pulse width	20 ns
Maximum Set-point Value	65,535 (16 bits)
Output Connector Types	Single-pin LEMO receptacle, shell size 00
Mating Connectors	KineticSystems Model 5910-Z1A
Power Requirements	
+5 V	2.6 A, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-sized VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V645-LA11 8-channel Timing Pulse Generator, High-true TTL outputs
Model V645-LB11 8-channel Timing Pulse Generator, Low-true TTL outputs

Related Products

Model 5857-Axyz Cable—1-contact LEMO to Unterminated
Model 5857-Bxyz Cable—1-contact LEMO to 1-contact LEMO
Model 5857-Hxyz Cable—1-contact LEMO to BNC shielded
Model 5910-Z1A Connector—1-contact LEMO

UNPACKING AND INSTALLATION

The Model V645 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V645 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V645 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. (Refer to FIGURE 1.)

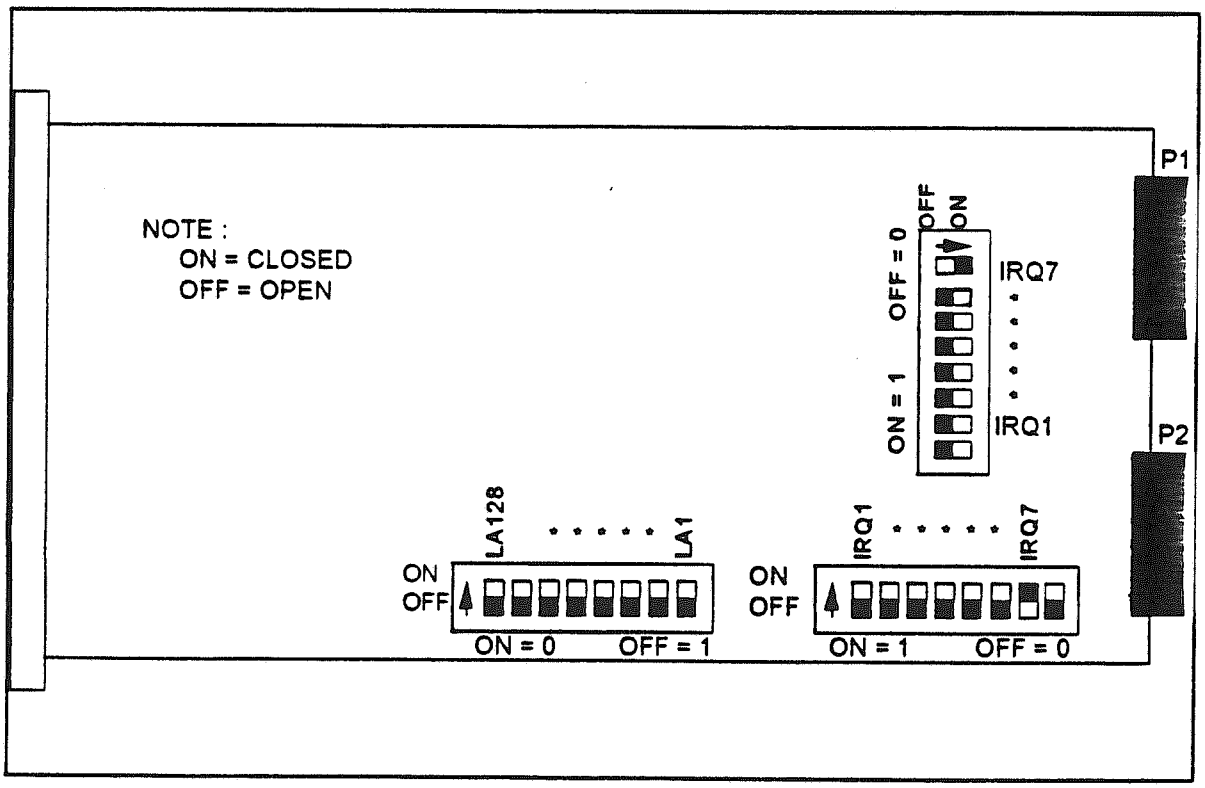


FIGURE 1 - V645 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to "1" (VXI defined).

Bits 13 through 6 are user-selectable via the address switches LA128-LA1.

Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V645 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 (page 3) for the switch locations and switch settings. Both banks of eight-position switches must be set to the same positions. As shown in Figure 1 (page 3) IRQ 7 is set to the same position in both banks.

Module Insertion

The V645 is a C-sized, single width VXIbus module. It requires 2600 milliamperes of +5 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame.

```
CAUTION:    TURN MAINFRAME POWER OFF WHEN
            INSERTING OR REMOVING MODULE
```

```
WARNING:    REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN
            JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE
```

To insure proper interrupt acknowledge cycles from the V645 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V645 and the Slot 0 Controller.

FRONT PANEL INFORMATION

LEDs

ADD_REC This LED is illuminated when the operational registers are being accessed.

INT SRC	This LED turns on when any one of the six channels has set its interrupt status bit.
1-8	These six LEDs indicate which channels are currently active.

CONNECTORS

1-8	These six single-pin LEMO connectors are the outputs to channels 1 through 8. Depending on the order option, these signals are either high-true (-LA11)or low-true (-LB11) TTL level signals which are 200 nanoseconds in width.
RECY	A single-pin LEMO connector is provided to allow external input of a start pulse signal. This Signal must be a TTL low-true signal at least 200 nanoseconds in length.Counting begins on the rising edge of the signal.
CLK	A single-pin LEMO connector is provided to allow an external input of a clock signal. This Signal must be a TTL signal. The maximum clock input frequency is 25 MHz, with a 50% duty cycle. The falling edge of the signal constitutes one tick of the clock.
INHIBIT OUT	A single-pin LEMO connector is provided to allow connection to an inhibit signal. This signal is an open collector type and will require an external pull-up. The output is a low-true signal.

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V645 implements those required for register-based devices. The V645 also contains a set of Operational Registers to monitor and control the functional aspects of the devices. Both registers sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range (C000 hex to FFFF hex). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of C000 hex to FFC0 hex.

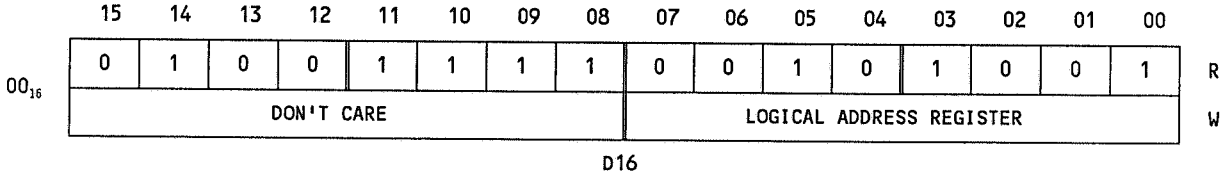
VXIbus Configuration Registers

Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V645 are offset from the base address. **Note: the V645 only responds to these addresses if the Short Nonprivileged Access (29 hex) or Short Supervisory Access (2D hex) Address Modifier Codes are set for the backplane bus cycle.** Table 1 shows the applicable Configuration Registers present in the V645, their offset from the base (Logical) address, and their Read/Write capabilities.

TABLE 1
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET (HEX)	W/R MODE	REGISTER NAME
00_{16}	W/R	ID/Logical Address Register
02_{16}	R	Device Type Register
04_{16}	W/R	Status/Control Register
06_{16}	W/R	Offset Register
08_{16}	R	Attribute Register
$1E_{16}$	R	Subclass Register

ID/Logical Address Register



On READ transactions:

Bit(s)	Mnemonic	Meaning
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V645. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

Device Type

02_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	1	1	0	1	1	0	0	1	0	0	0	1	0	1	R

On READ transactions:

Bit(s)	Mnemonic	Meaning
15 - 12	Required Memory	The V645 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model V645 (645_{16}).

Status/Control Register

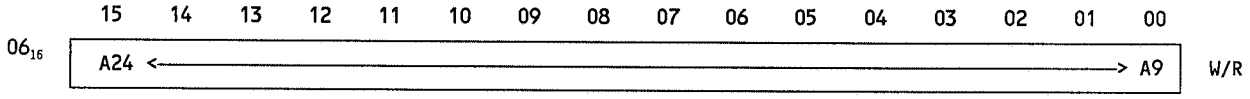
04_{16}

15	14	13	12	11 10 09 08 07 06 05 04	03	02	01	00
A24 ACT	MODID	S	1	ZEROs	RDY	PASS	0	RST
A24 ENA	N/U	N/U	1	NOT USED				RST

Bit	Mnemonics	Description
15	A24	Writing a "1" will enable A24 addressing and allow access to the Operational Registers. Reading a "1" indicates A24 is active. This bit is reset to a "0" on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on VXIbus connector P2. A "0" will indicate that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V645. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1".
11-4	N/U	Not used. Read as a "0".
3	RDY	READY. The V645 is always ready. Read as "1".

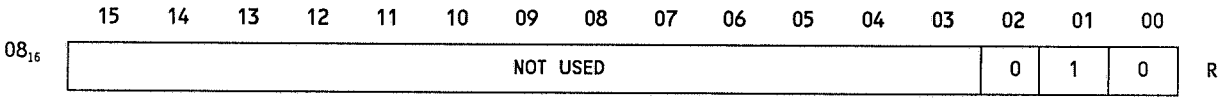
2	PASS	PASS. The V645 will always pass self tests. Read as "1".
1	N/U	NOT USED. Read as "0".
0	RST	RESET. This Read/Write bit controls the Soft Reset condition within the V645. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Registers (see below) except the Diagnostic and Interrupt Status registers is inhibited. The output bit patterns from the module are maintained in the state they were in just prior to the Soft Reset being enabled. This bit can be reset by writing a "0", on power-up or the assertion of SYSRESET*.

Offset Register



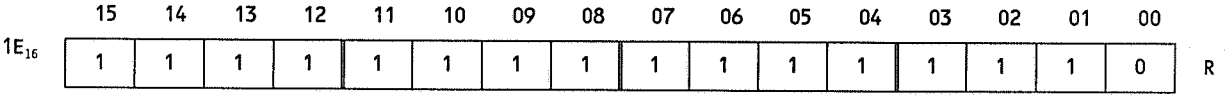
This 16-bit read/write register defines the base address of the A24 Operational Registers. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Attribute Register



Bits 3-15:	Not Used. Read as zeros
Bit 2 = 0	Indicates Interrupt Control Capability
Bit 1 = 1	Not an Interrupt Handler
Bit 0 = 0	Indicates Interrupt Status Capability

Subclass Register



Bit 15 = 1	Indicates that this is a VXIbus-defined Extended Device
Bits 14-0 = $7FFE_{16}$	Indicates that this is an Extended Register Based Device

OPERATIONAL REGISTERS

The Operational Registers are the means to access the functional registers of the V645. For compatibility with other KineticSystems VXIbus modules in this series, these registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set (page 7).

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register (see page 6). **Note: The V645 will only respond to these addresses if the Standard Nonprivileged Data Access (39 hex), Standard Nonprivileged Program Access (3A hex), Standard Supervisory Data Access (3D hex), or Standard Supervisory Program Access (3E hex) Address Modifier Codes are set for the bus cycle(s).**

Of the 256 bytes requested by the setting of the Device Type register in the Configuration Register set, only 62 bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type register.) Table 2 shows the applicable Operational Registers present in the V645, their offset from the base A24 address, and their Read/Write capabilities.

TABLE 2
V645 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

A24 OFFSET	W/R MODE	REGISTER NAME
00_{16}	W/R	Diagnostic Register
02_{16}	W/R	Interrupt Status/ID Register
12_{16}	R	Read Channel #1 Set Point
16_{16}	R	Read Channel #2 Set Point
$1A_{16}$	R	Read Channel #3 Set Point
$1E_{16}$	R	Read Channel #4 Set Point
22_{16}	R	Read Channel #5 Set Point
26_{16}	R	Read Channel #6 Set Point
$2A_{16}$	R	Read Channel #7 Set Point
$2E_{16}$	R	Read Channel #8 Set Point
32_{16}	W	Write Channel #1 Set Point
36_{16}	W	Write Channel #2 Set Point
$3A_{16}$	W	Write Channel #3 Set Point
$3E_{16}$	W	Write Channel #4 Set Point
42_{16}	W	Write Channel #5 Set Point
46_{16}	W	Write Channel #6 Set Point
$4A_{16}$	W	Write Channel #7 Set Point
$4E_{16}$	W	Write Channel #8 Set Point
52_{16}	W	Cycle Control Register
56_{16}	W	Inhibit Control Register
$5A_{16}$	W	INT Mask Register
$5E_{16}$	W	Read INT Status Bits
62_{16}	R	Clear and Enable the Counters and Begin counting
66_{16}	R	Inhibit Out Enable
$6A_{16}$	R	Inhibit Out Disable

A24 OFFSET	W/R MODE	REGISTER NAME
$6E_{16}$	R	Clear and Enable Counter and Clear the INT Status Bits
72_{16}	R	Clear INT Status Bits

Diagnostic Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care								D	S	0	INT ENA	INT SRC	0	0	0	R
00_{16}	Don't Care								0	0	0	INT ENA	0	0	CLR	INIT	W

Bit	Mnemonic	Description
15-8	D/C	Don't Care. Read as "0".
7	Diagnostic	When this bit is set to a "1", the last register access to the operational registers (OFFSET 12_{16} through $6A_{16}$) was valid.
6	Status	When this bit is set to a "1", the last register access to the operational registers (OFFSET 12_{16} through $6A_{16}$) was accepted.
5	N/U	Not Used. Read as "0".
4	INT ENA	Interrupt Enable: setting this bit to a "1" will enable interrupts.
3	INT SRC	Interrupt Source: When this bit is set to a "1", a channel on the V645 has reached its trigger point.
2	D/C	Don't care. Read as "0".
1	CLR	Setting this bit will clear the interrupt status bits.
0	INIT	Setting this bit to a one will only reset the operational registers (OFFSET 12_{16} through $6A_{16}$). The configuration registers and the Diagnostic register are unaffected.

Interrupt Status/ID Register 02_{16}

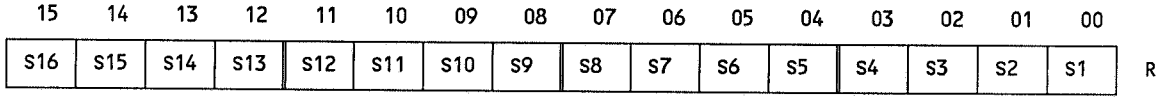
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	STATUS								ID								R

This is a read only 16-bit Interrupt Status Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.

Bit	Mnemonic	Description
15-8	STATUS:	These eight bits will indicate Request True or Request False: Request True = FD_{16} Request False = FC_{16}
7-0	ID:	These eight bits represent the Logical Address of the V645 Configuration Registers.

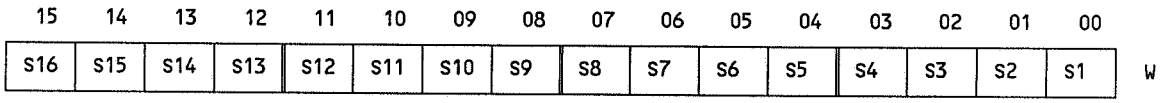
Read Channel Set Point Registers

Reading the Read Channel Set Point registers will return the set point data for the appropriate channel. The value returned indicates the number of counts of the time base which are required to occur before a pulse will be generated at the channel's output connector. These registers are located at offset addresses 12_{16} through $2E_{16}$.



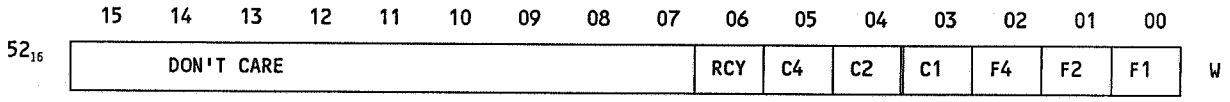
Write Channel Set Point Registers

Writing the Write Channel Set Point registers will set the appropriate channel's set point. The value written indicates the number of counts of the time base which are required to occur before a pulse will be generated at the channel's output connector. These registers are located at offset addresses 32_{16} through $4E_{16}$.



Cycle Control Register

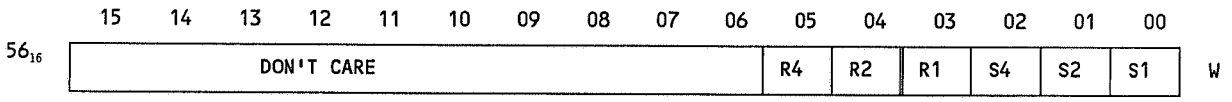
Writing the Cycle Control register will set the function parameters of the V645. The number of channels that will generate a pulse is selected with this register. The clock frequency as well as single shot or recycle mode are also selected by writing this register.



Bit	Mnemonic	Description
15-07	D/C	Don't Care. Reads as "0".
06	RCY	When set to a "1", this bit indicates that the V645 is in the recycle mode. When in this mode the V645 will continuously cycle through its sequence of set points. When this bit is set to a "0" the V645 will execute it's cycle once and stop.
05-03	C4-C1	These three binary-weighted bits are used to select the number of channels that will generate pulses. The number of channels to generate a pulse is computed using the following equation: C4, C2, C1 = P Number of channels = P + 1.
02-00	F4-F1	These three binary-weighted bits are used to set the clock frequency used for triggering the V645 counting sequence. The frequency to be used is determined by the following formula: F4, F2, F1 = N Freq = 10^N Hz (N = 7 selects the external clock input)

Inhibit Control Register

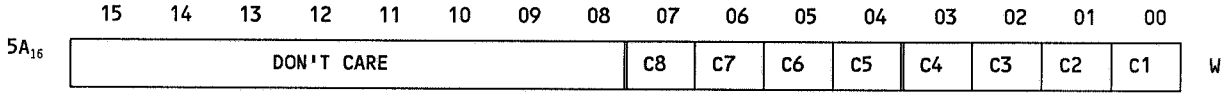
Writing this register will determine which channels will set and release the inhibit signal. The lower three bits will determine which channel will set the inhibit signal (0 = Channel 1, etc.). The next three bits will determine which channel will release the inhibit signal. A read of the Inhibit Enable register must be preformed for the inhibit signal to be generated.



Bit	Mnemonic	Description
15-06	D/C	Don't Care. Read as "0".
05-03	R4-R1	Release Inhibit 4 through 1 are used to select the channel which will release the inhibit signal. These three bits are binary weighted and contain a number which is one less than the desired channel number (i.e., R4, R2, R1 = 0 selects channel #1).
02-00	S4-S1	Set Inhibit 4 through 1 are used to select the channel which will set the inhibit signal. These three bits are binary weighted and contain a number which is one less than the desired channel number (i.e., S4, S2, S1 = 0 selects channel #1).

Write Interrupt Mask Register

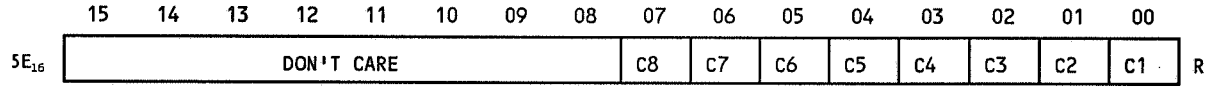
A write to this register will determine which channels are able to set the INT SRC (Interrupt Source) bit in the Diagnostic register.



Bit	Mnemonic	Description
15-08	D/C	Don't care. Read as "0".
07-00	C8-C1	These bits represent which channel can set the INT SRC bit in the diagnostic register. Writing a "1" to the appropriate channel's mask bit will cause that channel to set the INT SRC bit upon the channel's cycle completion. Writing a "0" to the channel's mask bit disables the channel's ability to set the INT SRC bit.

Read INT status Register

A read from this register will indicate which channels asserted the INT SRC bit in the Diagnostic Register.



Bit	Mnemonic	Description
15-08	D/C	Don't care. Read as "0".
07-00	C8-C1	These bits represent which channel has set the INT SRC bit. C1 indicates channel #1 has an INT SRC bit set. Likewise C8 indicates that channel #8 has set the INT SRC bit set.

OPERATIONAL CONTROL REGISTERS

The V645 has five Operational Control Registers at offset addresses 62_{16} through 72_{16}. These registers are Read-Only and return a 16-bit data code. There are only two possible codes that can be returned. The first data code will return a value of "0" and has the same meaning as the Status bit in the Diagnostic Register set to logical "0". The second data code will return a value of one and has the same meaning as the Status bit in the Diagnostic Register set to a logical "1". This data code will indicate the command was accepted or a test condition is true when equal to one. These five Operation Control Register are described below:

Clear and Enable/Begin counting (OFFSET 62_{16})

For every read from this register, the V645 counters will be cleared and enabled and counting will begin. This register will return a data code of one.

Inhibit Out Enable (OFFSET 66_{16})

A read from this register enables the ability of the module to assert the Inhibit signal. The signal will be asserted when the selected channel reaches the end of its cycle. This register will return a data code of one.

Inhibit Out Disable (OFFSET $6A_{16}$)

A read from this register disables the ability of the module to assert the Inhibit signal. This register will return a data code of one.

Clear and Enable counter and Clear the INT Status (OFFSET $6E_{16}$)

For every read from this register, the V645 will clear and enable all the channel counters and clear the Interrupt status bits, thus clearing the INT SRC bit in the diagnostic register. This register will return a data code of one.

Clear INT Status (OFFSET 72_{16})

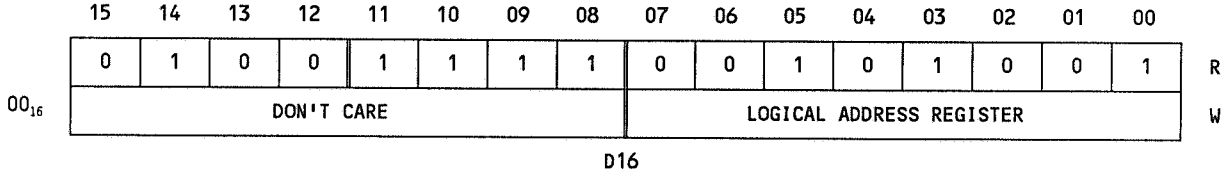
For every read of this register, the INT status bits will be cleared thus clearing the INT SRC bit in the diagnostic register. This register will return a data code of one.

APPENDIX

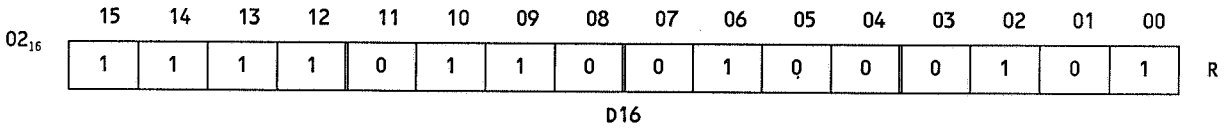
V645 REGISTER LAYOUT

CONFIGURATION REGISTERS

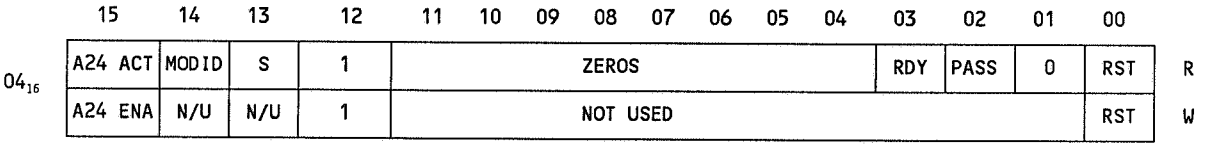
ID/Logical Address Register



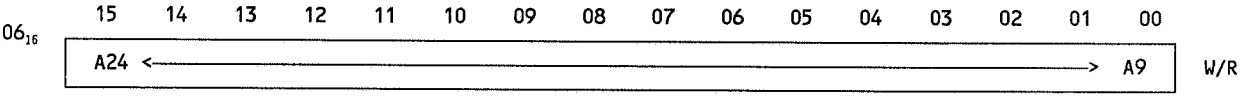
Device Type



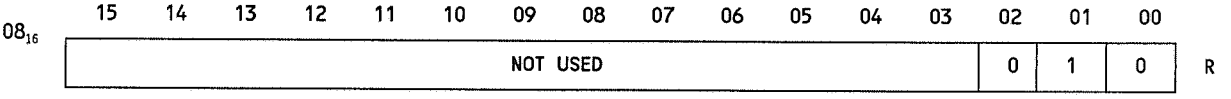
Status/Control Register



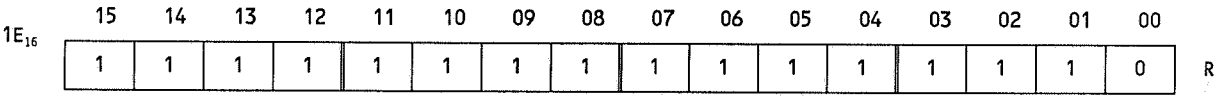
Offset Register



Attribute Register

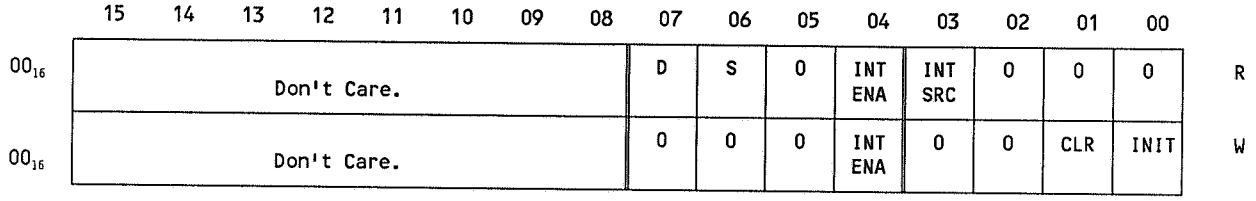


Subclass Register

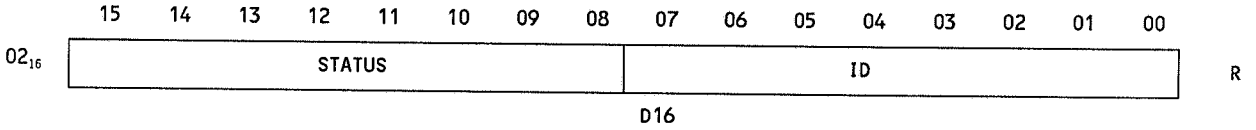


OPERATIONAL REGISTERS

Diagnostic Register

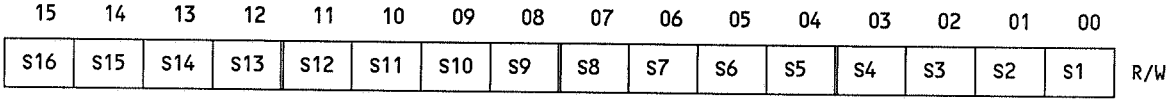


Interrupt Status/ID Register

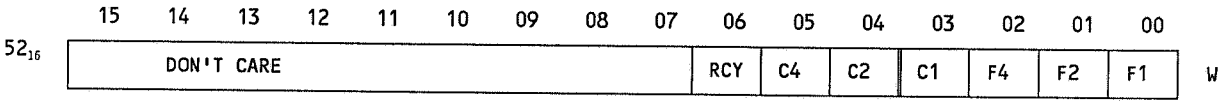


;ead Channel Set Point Register
7rite Channel Set Point Register

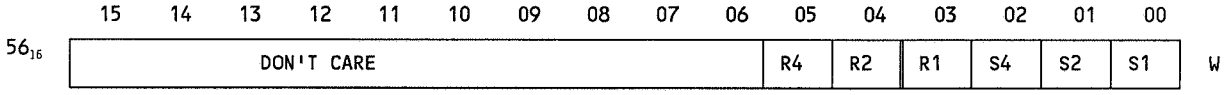
Channel	1	2	3	4	5	6	7	8
LOW	12_{16}	16_{16}	$1A_{16}$	$1E_{16}$	22_{16}	26_{16}	$2A_{16}$	$2E_{16}$
HIGH	32_{16}	36_{16}	$3A_{16}$	$3E_{16}$	42_{16}	46_{16}	$4A_{16}$	$4E_{16}$



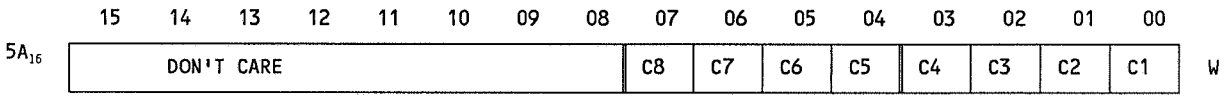
Write Cycle Control Register



Write Inhibit Control Register



Write Interrupt Mask Register



Read Interrupt Status Register