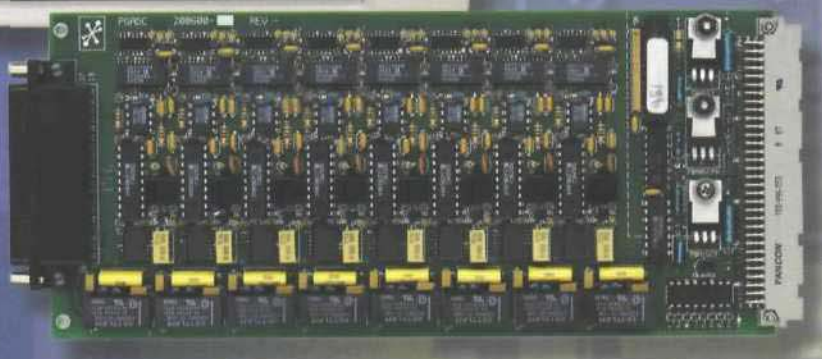
DPS...
PRESYS 1000mV
Data Processing System

PRESYS 1000mV

Dynamic Range of
5 mV to 10 Volts
Full Scale with
16 bit Resolution

Accuracy
System Features
Including:
120 dB CMRR
.01% Linearity
.5µV Zero TC
.005% Gain TC
.02% Accuracy



PRESTON

INTRODUCTION

PRESYS 1000mV combines many of the standard features of the PRESYS 1000 Data Conversion Systems with the new wide dynamic range high resolution DSC* input channel, the PGADC-824.

DESCRIPTION -

The **PGADC-824** is an 8 channel, low speed, wide dynamic range data acquisition card. Each channel consists of a differential low thermal relay to allow switching between the normal input of the system and a calibration bus. Following this switch is a differential input programmable gain stage offering buffering, high common mode rejection of 80 dB plus gain, a low pass normal mode input filter to reduce noise along with a low pass common mode filter to reject high frequency pickup which may become rectified and produce reading errors. Following this input stage is a 24 bit delta-sigma ADC. All control of this card is optically isolated from the digital world to improve measurement accuracy.

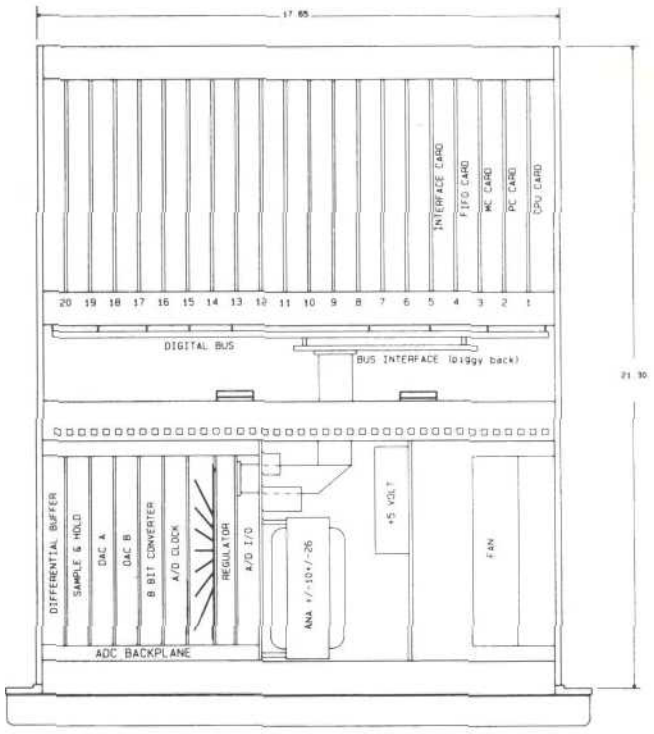
This card is designed to function along with the additional PreSys product options, thus it is possible to have digital input data (i.e. time code data) along with the ADC acquisition data, or multiple interfaces. Use of the Channel Address Memory (CAM) is possible for changing data order or removing a channel from the data stream. The **PGADC-824** *(Dalta Sigma Converter)* may reside also within a high speed system so the user can use the system for both high speed data and slow speed data.

THE SYSTEM -

PRESYS 1000, Preston's newest data conversion system is organized as an "Analog and Digital, Input and Output" Data Processing Sub-System that combines multi channel A/D Conversion, D/A Conversion, Digital Input and Output Multiplexing all in one easily interfaced Instrumentation Package.

The basic system includes space for high-speed A/D Converter, combined input/output DATA BUS featuring Analog Bus Structure for Analog inputs and Digital Bus structure for Digital Inputs and Digital Outputs {Memory expansion and multiple computer interfaces). Further the basic PRESYS 1000 System Chassis includes the UPC controller, 30k word channel address memory, 128k FIFO memory, basic computer interface, front panel control system and separate power supplies for Analog and Digital modules.

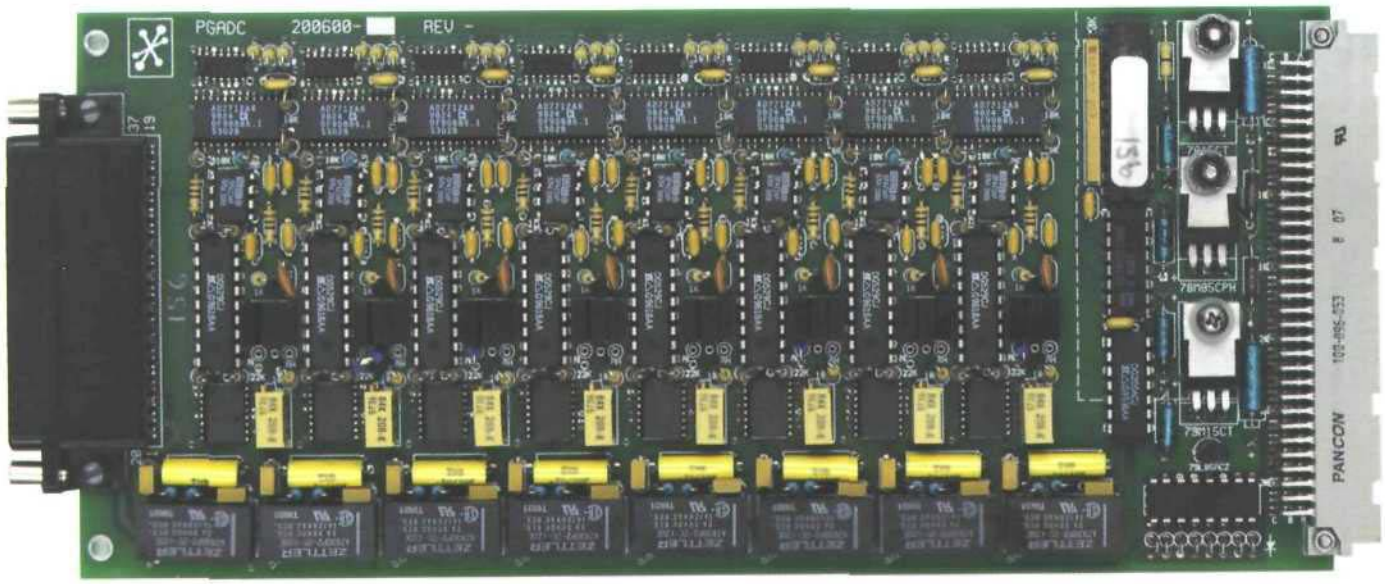
PRESYS 1000 Basic Chassis I/O Data Bus will accept up to 16 card modules which contain either Analog Input Channels, Digital Input Channels and/or Digital and Analog Output Channels (D/A Converters). This same Card space will also accept other System functions i.e., additional Computer Interfaces, FIFO expansion, Chassis expansion electronics (the logic necessary to attach the PRESYS 1000 Expansion Chassis), and any of the following Input or Output Channels or System Control Functions... Analog Multiplexer 16 Channels/Module, Sim



PRESYS 1000 Master Chassis

Sample-and-Hold 8 Channels/Module, Digital Inputs 16-64 Bits/Module, Digital Outputs 16-64 Bits/Module, Analog Outputs 1-4 Channels/Module, FIFO Buffer 128k to 1 Meg/Module, Computer Interface 1 or 2 Modules/Interface, and Bus Expansion 2 to 4 Modules/Chassis.

** Delta Sigma Converter*



PGADC-824 Typical 8 Channel Module

128 channels per chassis, expandable to 1024 channels per system

THE PGADC-824 CHANNEL -

The heart of a channel is the 24 bit delta-sigma converter. This converter has a fixed conversion rate of 19.5KHz. The ADC has a programmable digital notch filter which determines the output data rate and filters the noise to achieve a 24 bit result. The possible data rates are from 9.76Hz to 119.82Hz. Rates up to 1KHz are possible with some loss in system performance. Rates below 9.76Hz are possible as a special non-standard operating option. When notch frequencies of 10, 30 and 60 are chosen, 60Hz noise is dramatically reduce to more than 150 dB. Notch frequencies of 10, 25 and 50 dramatically reduce 50Hz noise to more than 150 dB.

The overall response of the filtering components, the front end single pole along with the digital filtering yield a roll off of 24 dB per octave, with high attenuation notches at multiples of the programmed notch frequency.

The delta-sigma converter includes a programmable gain function. The gains used from this converter to give optimum performance are 1, 2, 4 and 8. Preceding the converter is a programmable gain amplifier. This amplifier is programmed to a gain of 1, 16 or 256 to achieve overall gain settings of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024 and 2048.

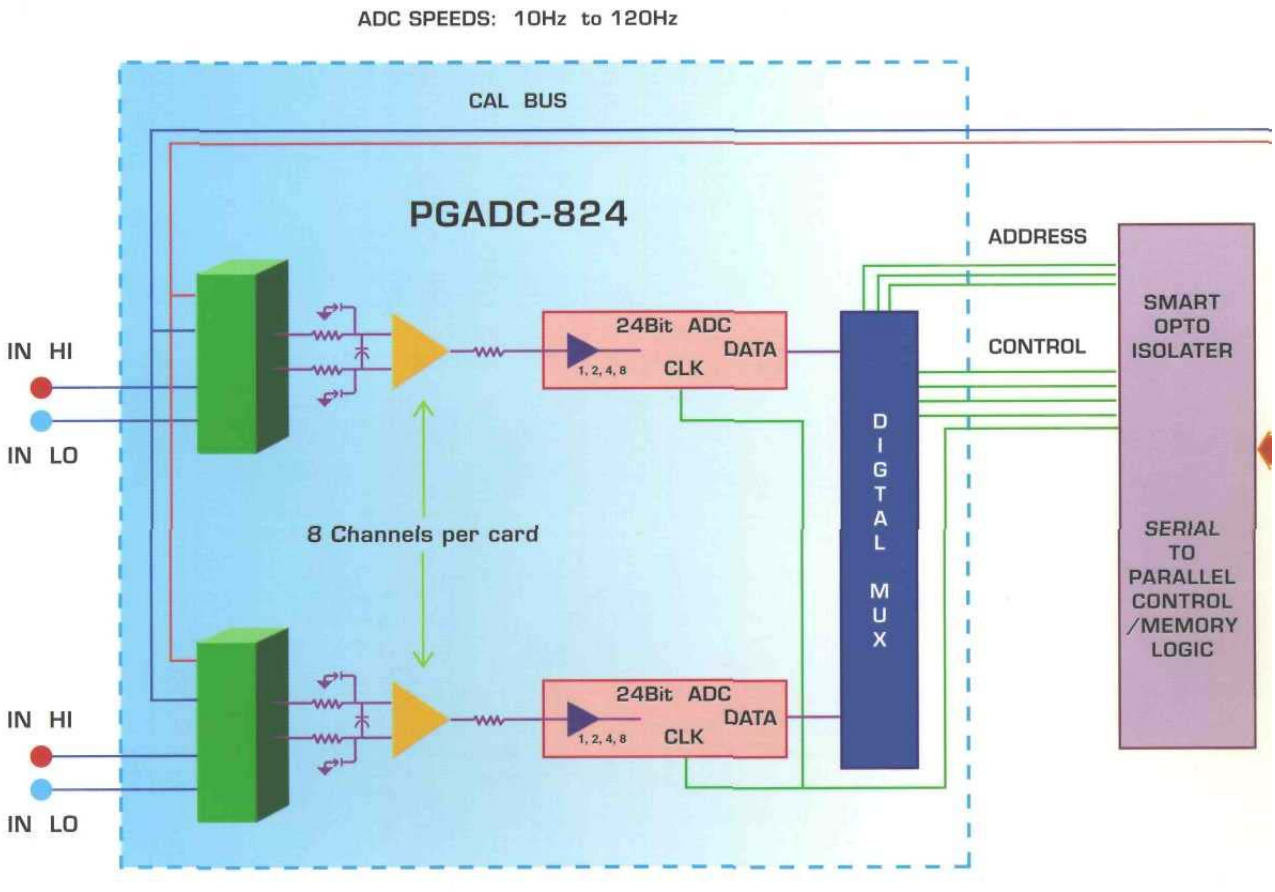
To achieve the 8 channel card density, an additional card common to all channels within a chassis (the Smart Opto card) is present and is used for all control logic, data shifting, serial to parallel converting, parallel to serial converting, channel gain memory, and PreSys bus protocol logic for communicating to the systems FIFO/INTERFACE and CPU.

CALIBRATION -

The system includes an internal calibration bus to correct for system offsets and gain errors. During calibration,

Values are stored on a per channel basis to correct the channel for system offset and gain errors.

PGADC-824 SYSTEM



PROGRAMMING -

Programming gain is made simple. Programming is done in the same manner as programming the PreSys CAM table. The user sets up a range of channels to program. This is done by sending to the PreSys system a first channel and last channel. This data is then followed directly with the list of gain codes for the channels selected. The system will then take the gain code sent and break it up into two pieces, one part for the ADC's input PGA, and the other part for ADC itself to achieve the desired overall gain.

System gain	Gain Code	Input PGA Gain	Gain of ADC
1	0	1	1
2	1	1	2
4	2	1	4
8	3	1	8
16	4	16	1
32	5	16	2
64	6	16	4
128	7	16	8
256	8	256	1
512	9	256	2
1024	10	256	4
2048	11	256	8

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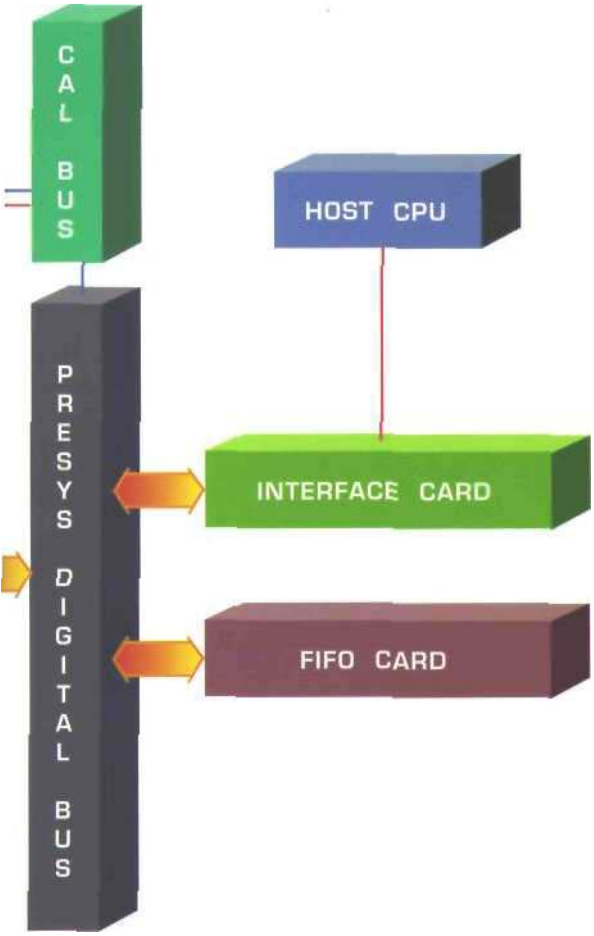
Programming the notch filter (ADC data output rate) is done in the same manner as programming a PreSys scan clock.

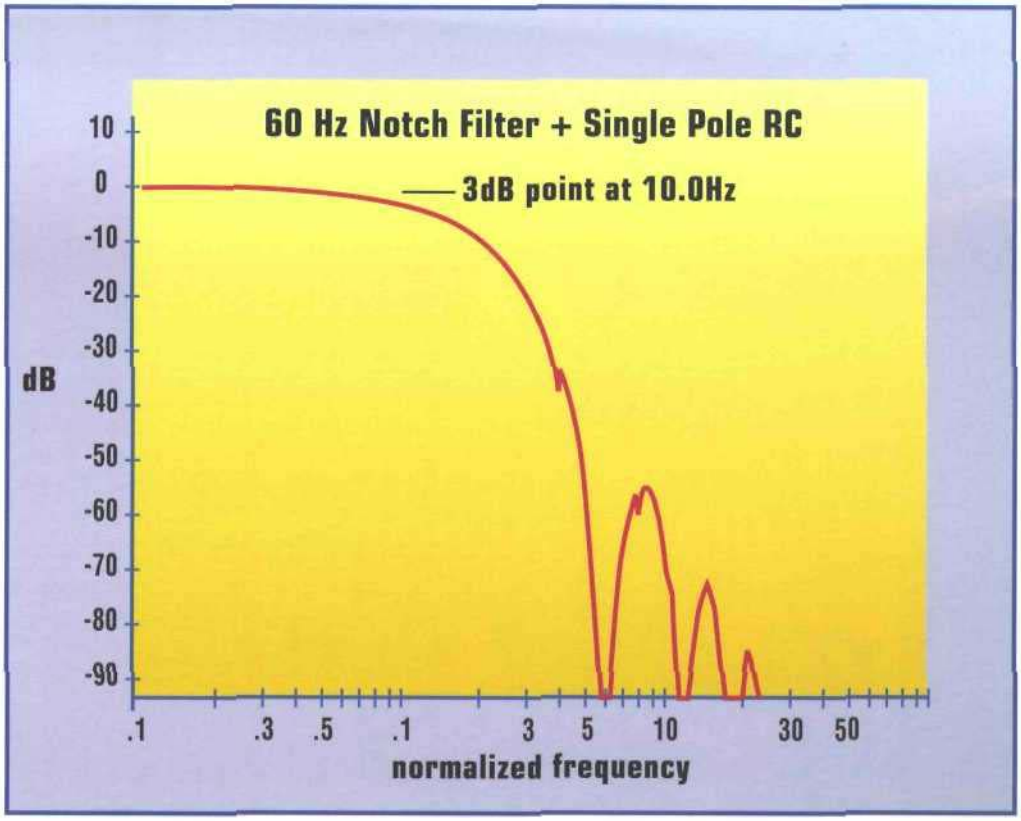


SPECIFICATIONS -

Number of Channels	8 true differential input channels per card. 128 channels per chassis. Expandable to 1024 channels.
Channel to Channel Cross Talk Isolation	126 dB (DC to 120Hz).
Input Configuration	Balanced, differential.
Input Impedance	Greater than 100 megohms min at DC shunted by 1000 pf max.
Bias Current	1nA typical 2nA max, .05nA/degree C
Maximum Input Voltage	±40V without damage, common mode or differentially.
Common Mode Rejection	80 dB plus gain in dB to 120 dB dc to 60Hz with 350 ohms of source imbalance, (notch freq. = 119.82)
Common Mode Voltage	±10V operating.
RF Rectification Rejection	94 dB (10KHz to 900KHz) 102 dB (1MHz to 20MHz)
Channel Sample Rate	Programmable rates. 9.76Hz to 119.82Hz to meet all specs.
Full Scale Ranges	±5mV to ±10.24V in 12 steps.
Warm-up Time	60 minutes
Accuracy (before warm-up)	±0.05% FS ±10µV RTI
Accuracy After Cal	±0.02% FS ±2µV RTI
Linearity	±01%
Zero TC Stability	±.5µV RTI ±.05mV RTO per degree C
Gain TC Stability	±.005% per degree C
ADC Resolution	15 Bits plus Sign (16 Bits)

NOTCH FILTER

Shown is typical GOHz Notch Filter. The Notch Filter is set as result of the programmed data rate from 9.76Hz to 1KHz. Programming the Notch Filter is done in the same manner as programming the PreSys Scan rate clock.



DIAGNOSTIC FUNCTIONS -

This self-checking system operates to provide two types of performance verification:

1 - It periodically tests the correct operation of the PRESYS 1000's internal data conversion and handling circuits, to verify that all sub-systems are performing correctly, and -

2 - It can deliver a sequence of test signals to the host computer that will demonstrate that all aspects of the digital interfaces between the computer and the PRESYS 1000 System are operating correctly.

To verify that both the host computer and the PRESYS 1000 System are operating correctly, a test signal can be programmed through the test sequence software that will verify - through the computer's display or printout - that all of the resulting data is correct, thereby confirming that all of the test system's equipment interfaces - and their sub-system components - are operating correctly.

This system can also verify that the customer's program software is properly functioning in the single-channel and multichannel modes, and that there are no unexpected 'cross-talk' conditions.

A bright red light on the PRESYS 1000's front **panel** provides the indication of incorrect performance. A 'call-up' instruction from the front panel controls will produce a coded indication of where in the system the 'error' was detected, allowing the source of the fault to be immediately located and corrected.

The PRESYS 1000 System's self-diagnostic procedures can test FIFO, Channel Address table (CAM), UPC Controller functions, first-last channel and control modes, and facilitates testing of the accuracy and timing of the A-to-D converter.

This built-in diagnostic capability operates by simulating the A-to-D converter's output data (from 16 bit counters) and outputting it to test the logic protocol, the bus protocol, the internal cabling, opto-isolator circuits, FIFO and interface electronics.

The PRESYS 1000 System's diagnostic capability also provides a 'power-on' verification of the system's internal timing circuits, logic sequencing and field addressing functions.

THE PRESTON INTEGRATOR

DATA ACQUISITION INTERFACE HARDWARE & SOFTWARE -

The Preston Integrator is a program designed to make the task of testing a PreSys System or use of the system an easy one. The program in it's original form will allow the user to run many of the different diagnostic tests available. Some of these tests will display information about the system like, number of channels and types of boards installed, whife other tests check the system for proper functioning, like the FIFO Echo test. This test outputs a data pattern from the Host computer to the PreSys System, and echoes it back to the Host through the PreSys FIFO. These diagnostic tests give the user confidence that their equipment is working correctly.

The Preston Integrator package consists of a group individual programs that are all orchestrated by one. The integrator, the program name "Preston", is a program that allows the user to fill out various windows of information and invoke the many different programs present.

These individual programs can be invoked from outside of the integrators environment. When this is done a command line argument is added after the program name so the proper Test Set information can be passed to the program. These programs along with their source code allows the user to tailor this package to meet their needs.

Preston Integrators are available for either PIF-488 Interface or the P-SCSI-2 Hardware Software Interface.

PIF-488 is a hardware interface that is compatible with IEEE488 protocol combined with the Preston Integrator, the PIF-488 is software compatible with most National Instruments IEEE488 boards.

P-SCSI-2 is a hardware and software interface incorporating the BUS-Logic 545-S Interface module and cable. The P-SCSI-1/2 Interlace is ISA and 100% SCSI-2 Interface compatible and supports transfer rates to memory at data rates of 7 megabytes per second (ASYNC) and 5 megabytes per second (SYNC, SCSI-1) or 10 megabytes per second (SYNC, SCSI-2). The actual rates within the PreSys 1000 will be slower because the present PreSys 1000 sub-system will not transfer data this fast. Existing bench marks for PreSys 1000 have supported asynchronous transfers to the computer at 5MB/s rate from the PreSys 1000 FIFO Buffer.

The P-SCSI-2 Software includes drivers Handlers and trouble shooting routines for the interface.

Data Acquisition Software - The Preston Integrator provides drivers for integrating Labview, Dadisp and TestPoint DAS packages.